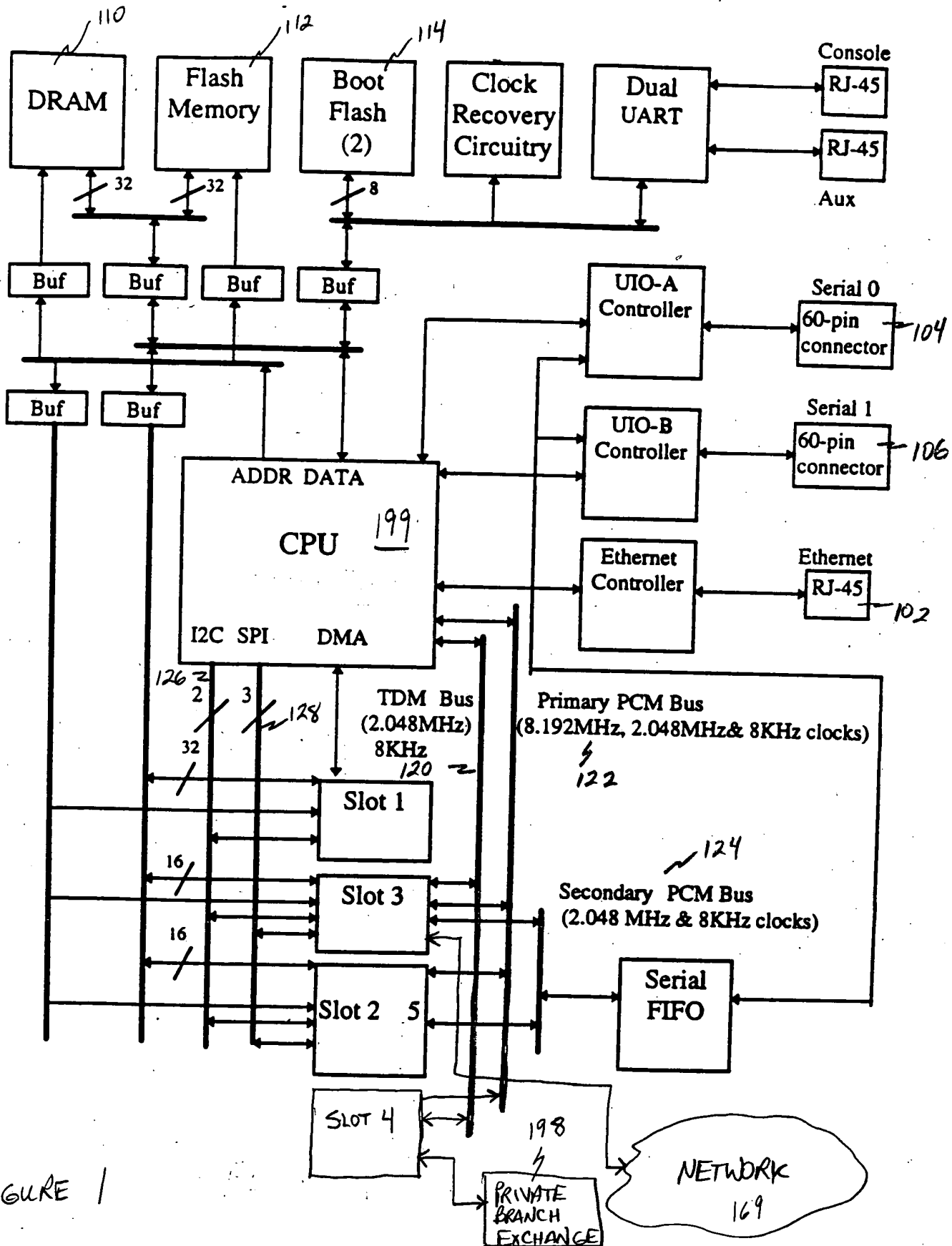


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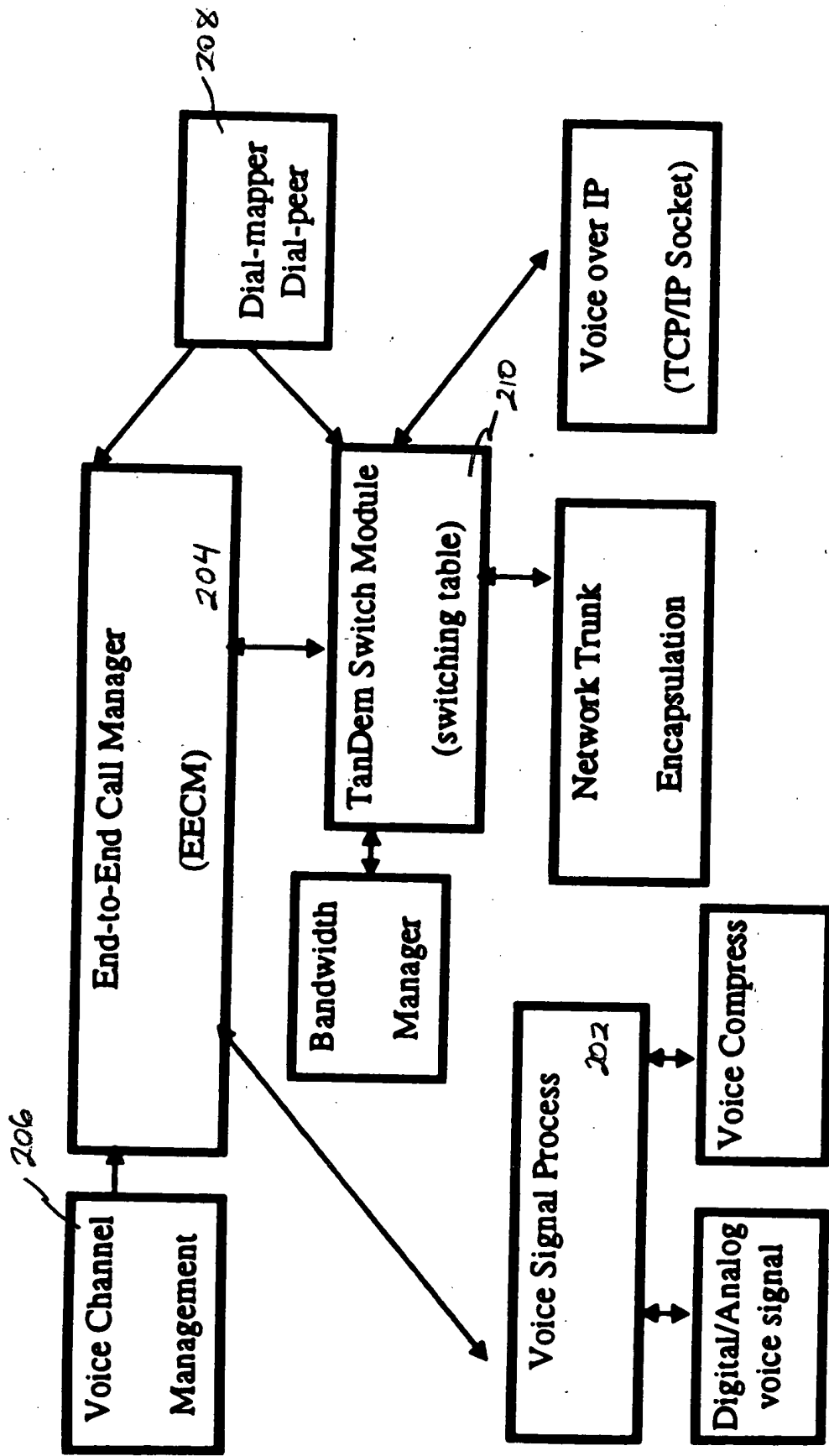


FIGURE 2

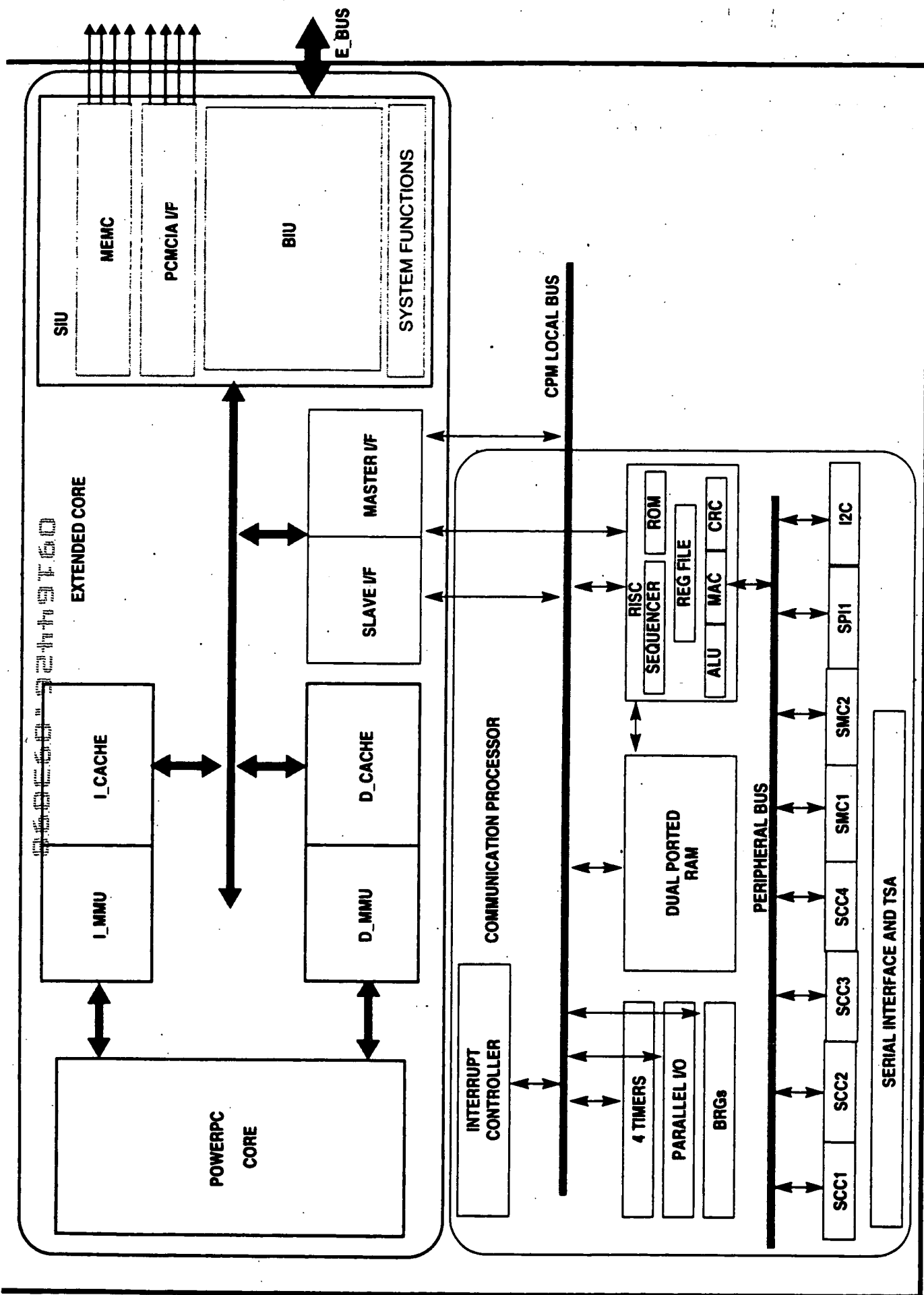


FIGURE 3

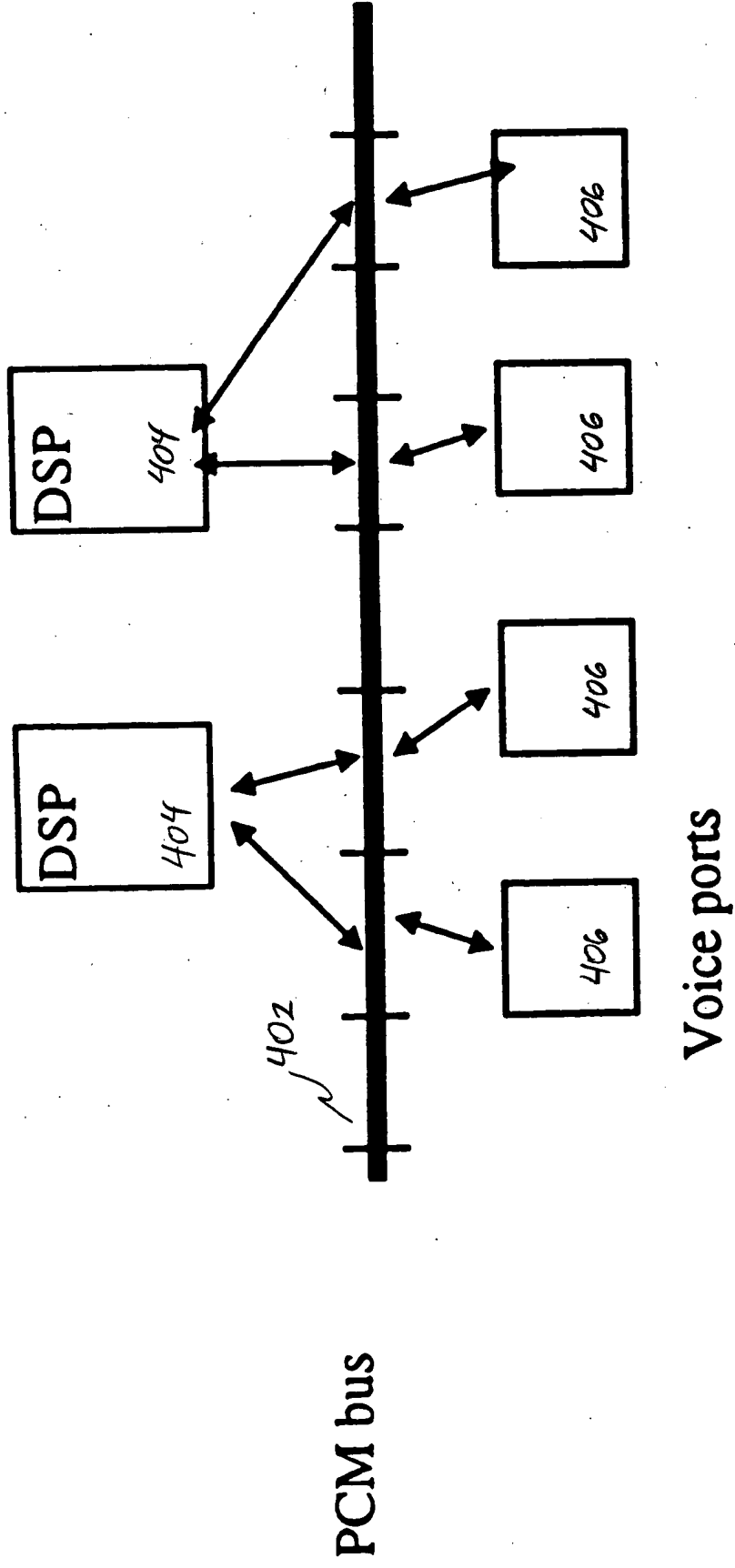


FIGURE 4

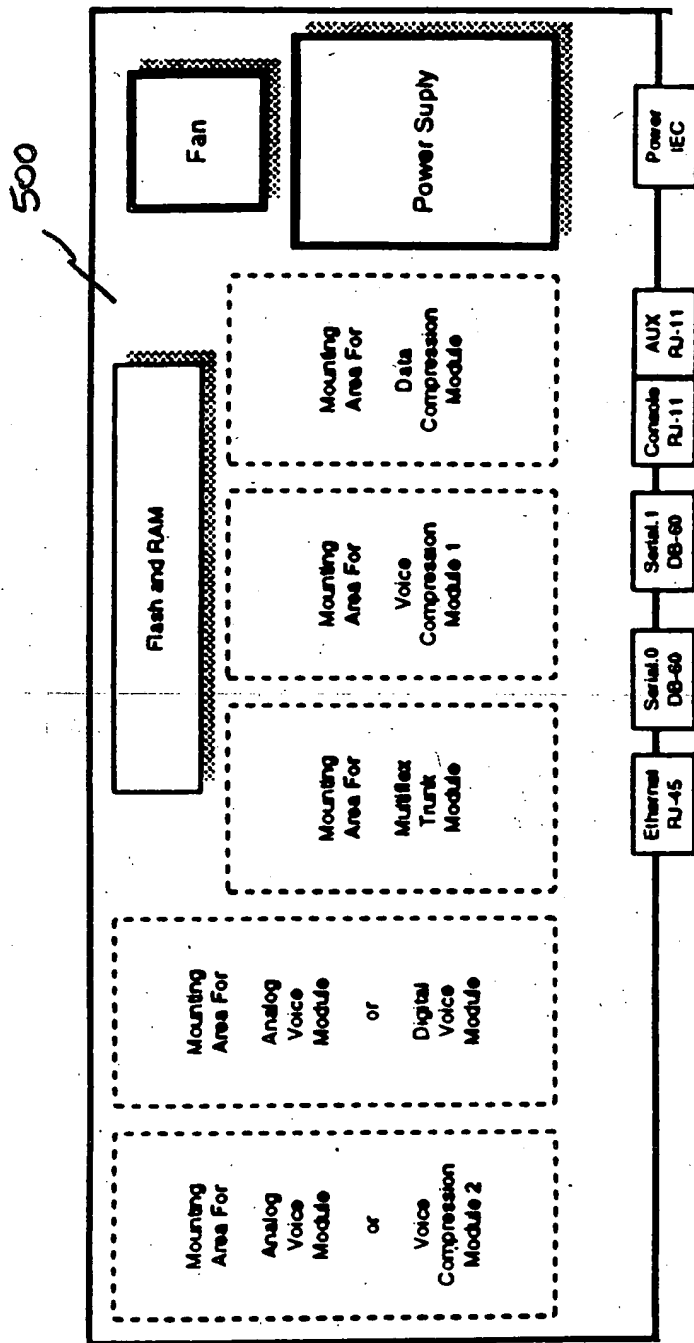


FIGURE 5

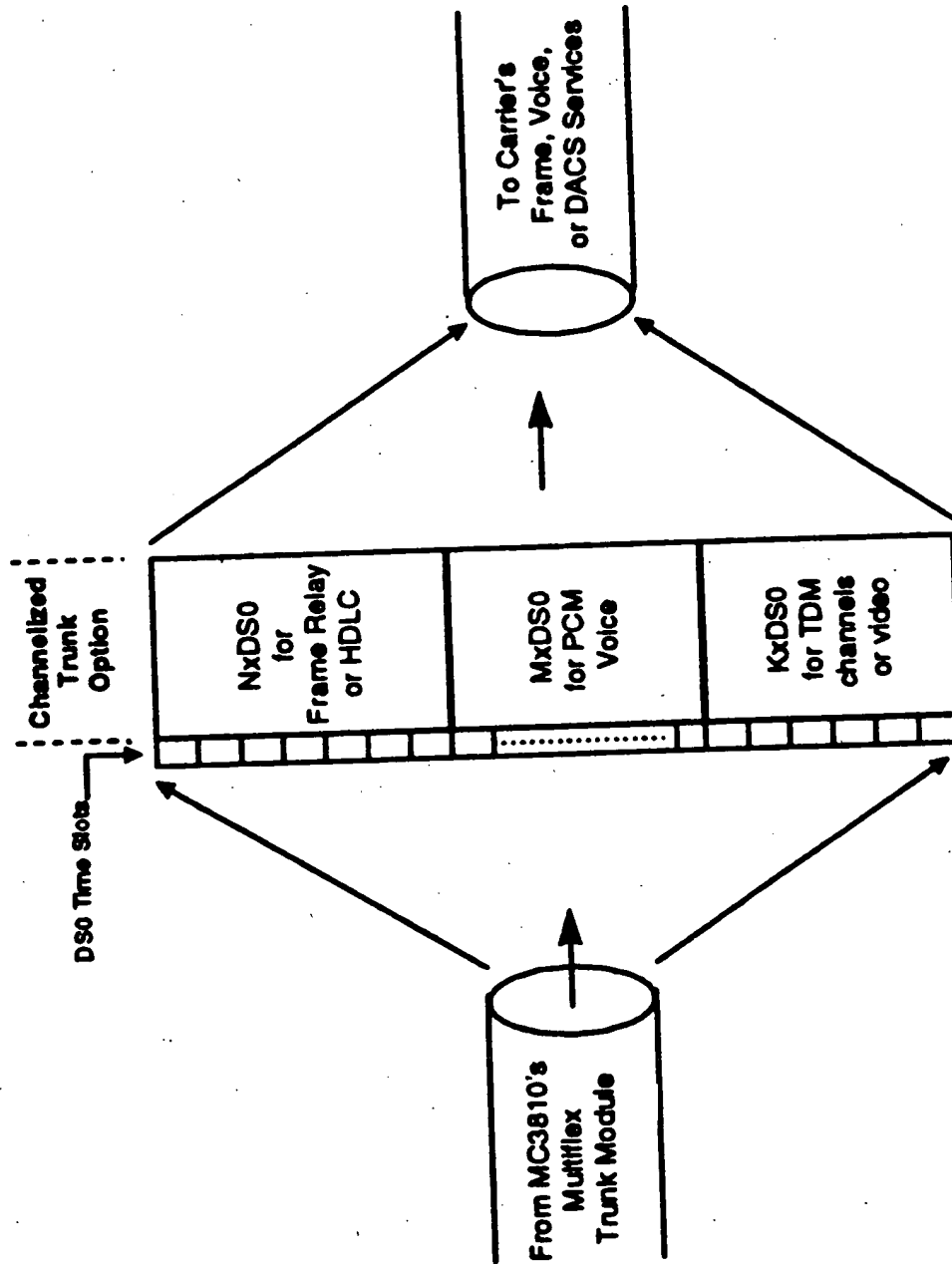


FIGURE 6

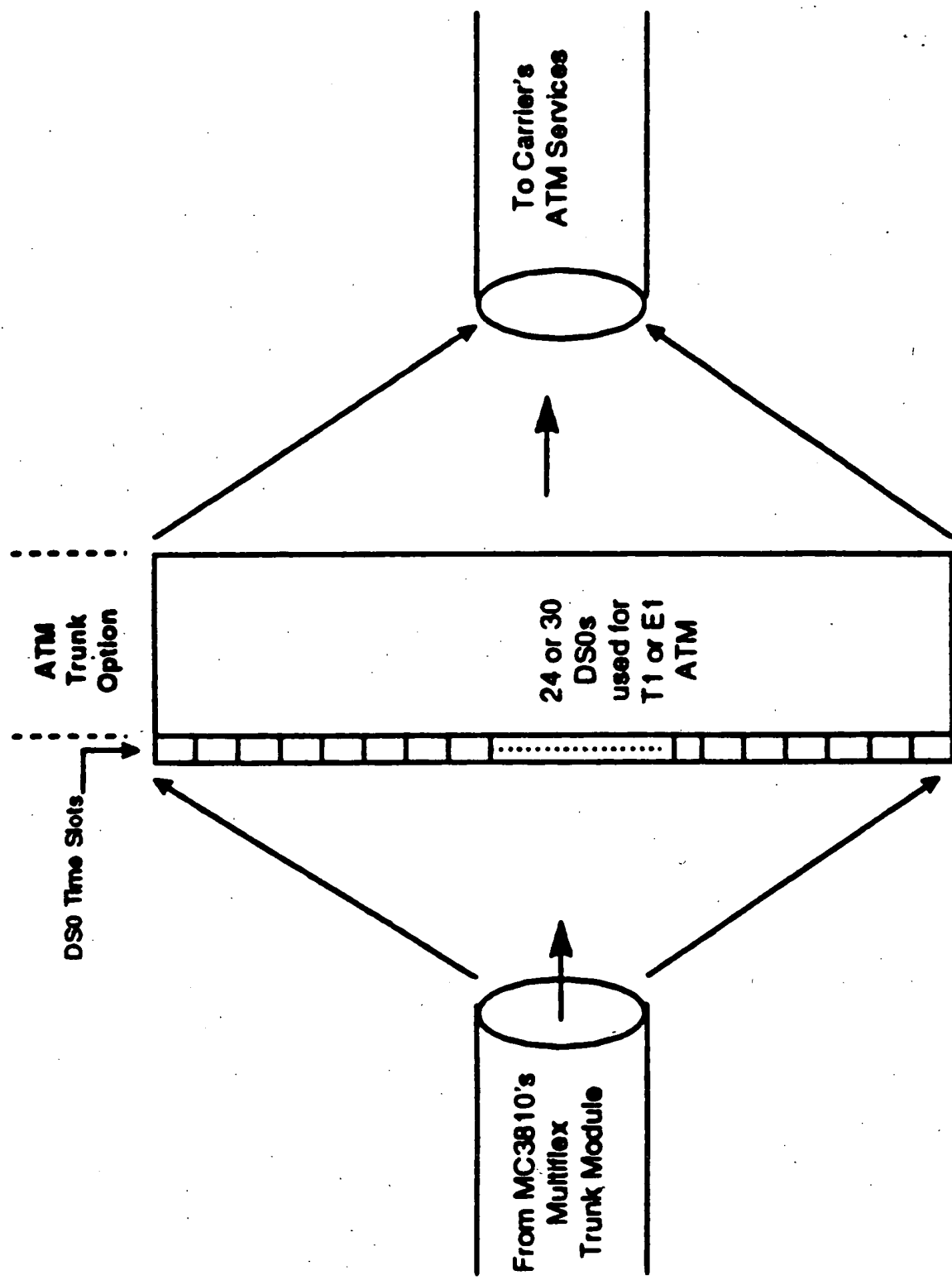


Figure 7

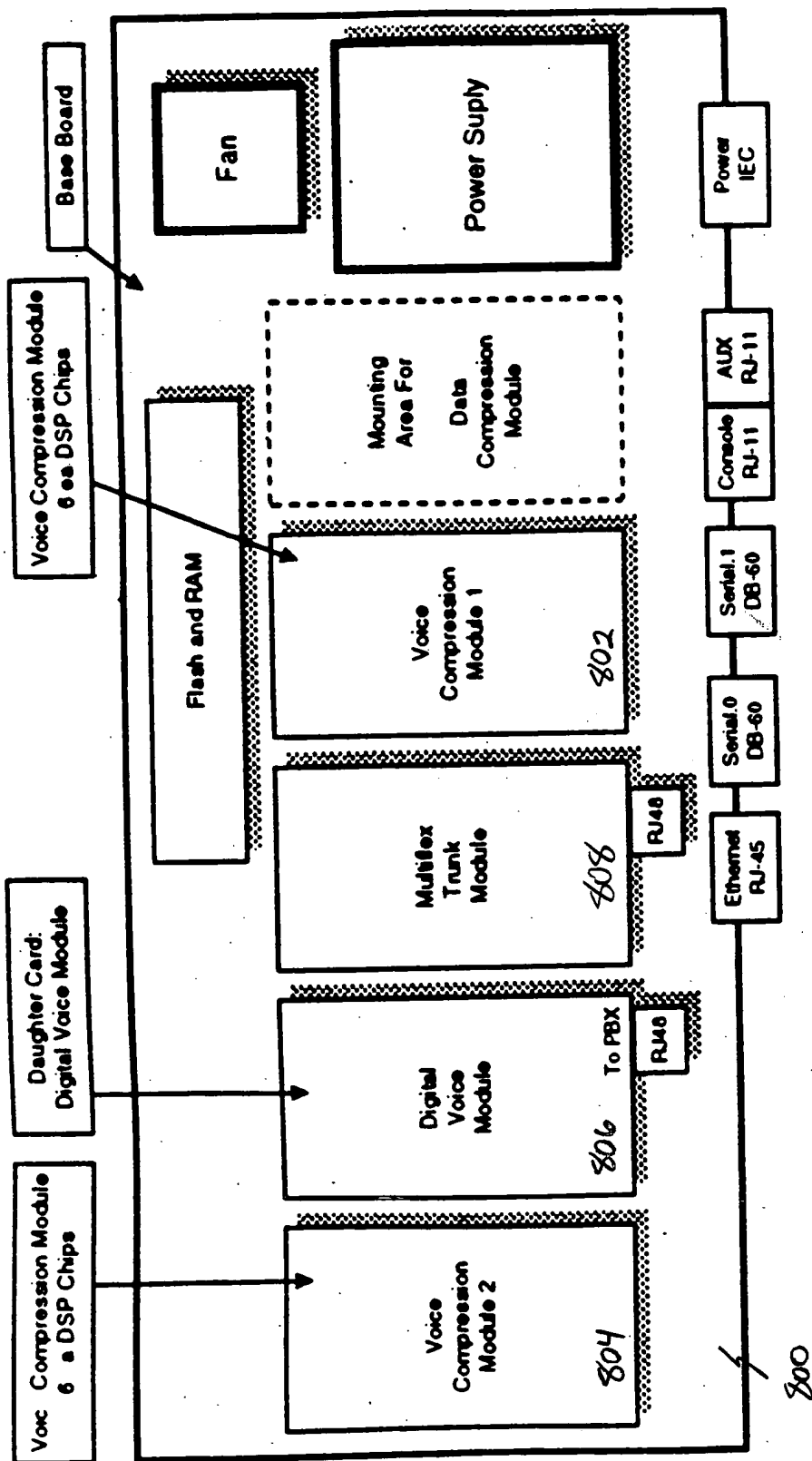


FIGURE 8

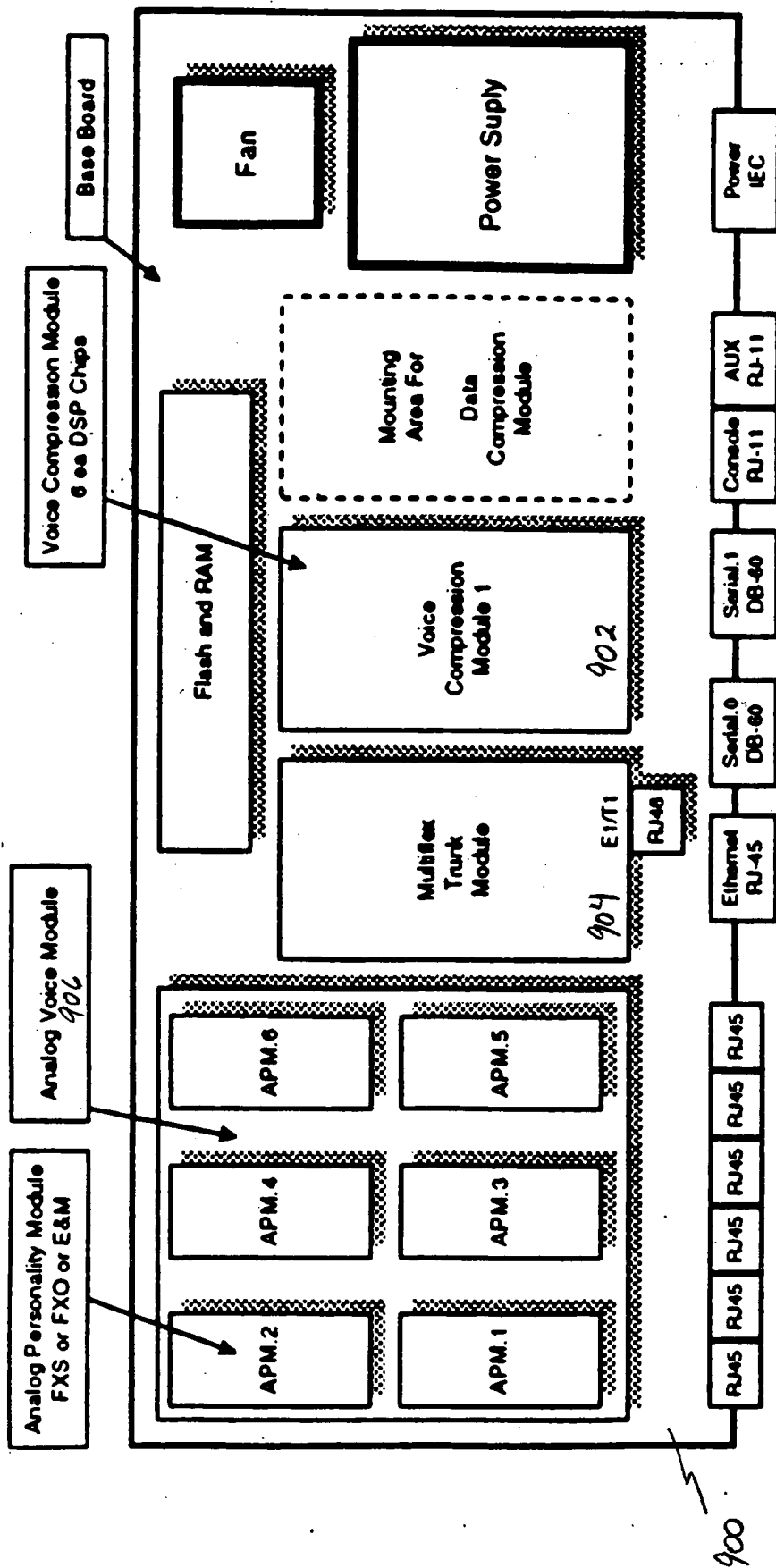


Figure 9

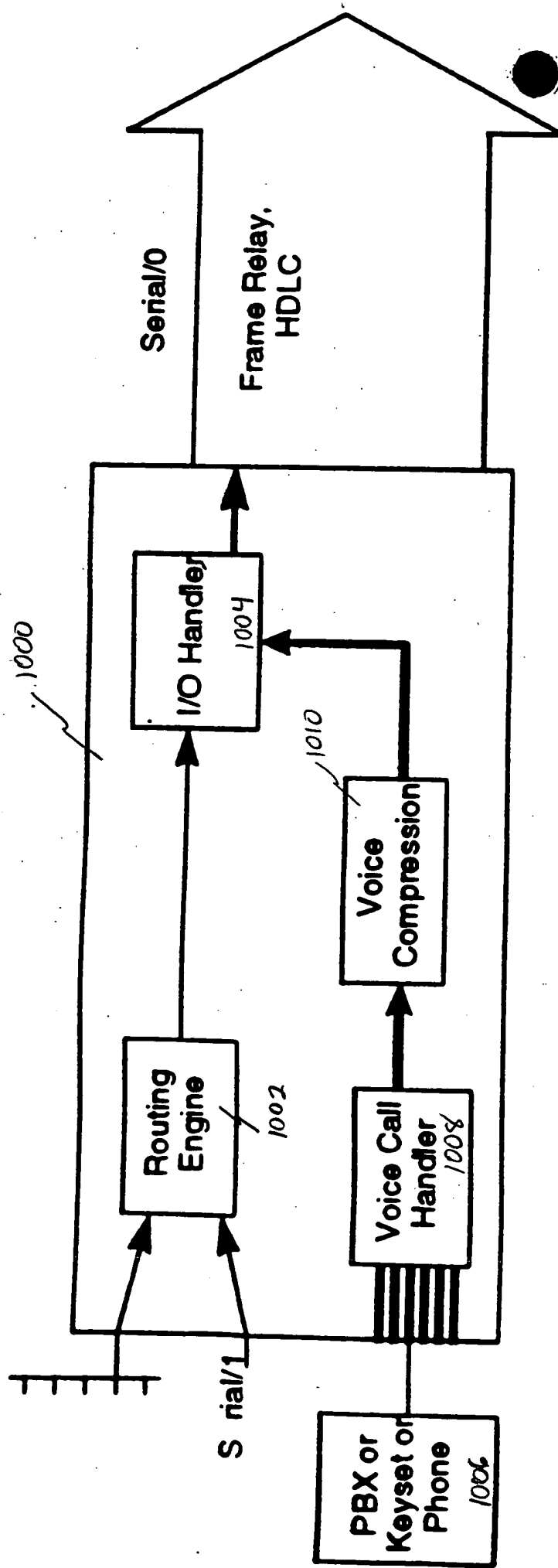


FIGURE 10

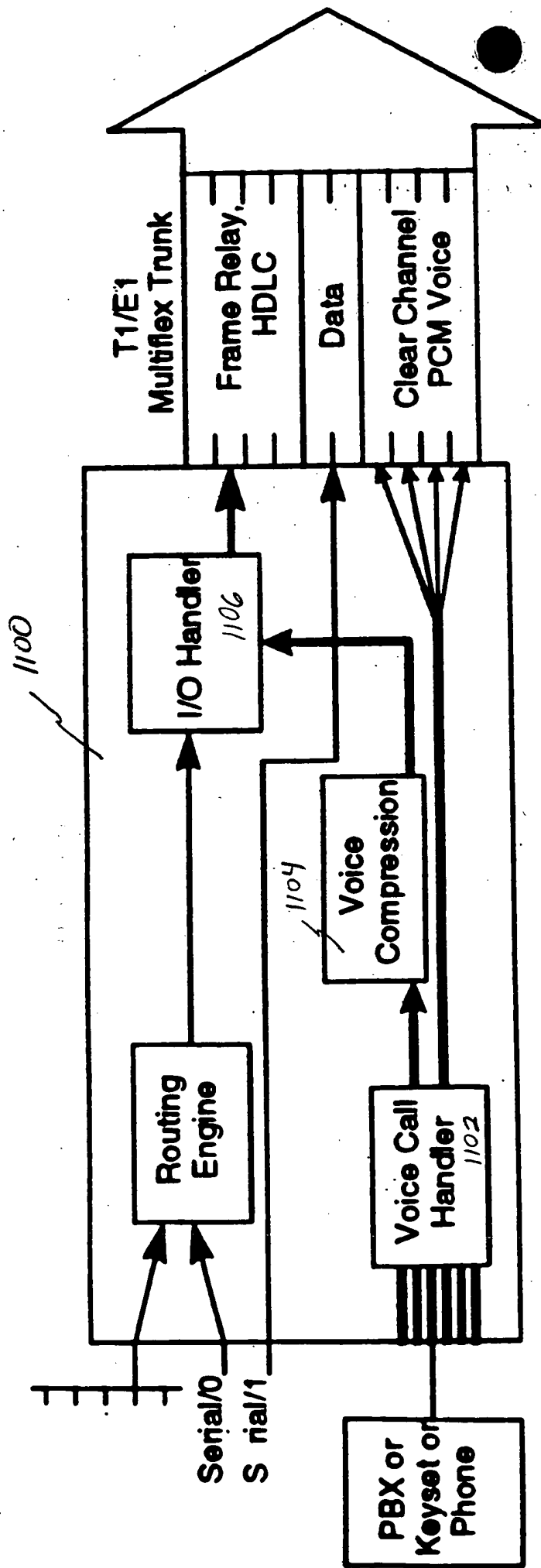


FIGURE 11

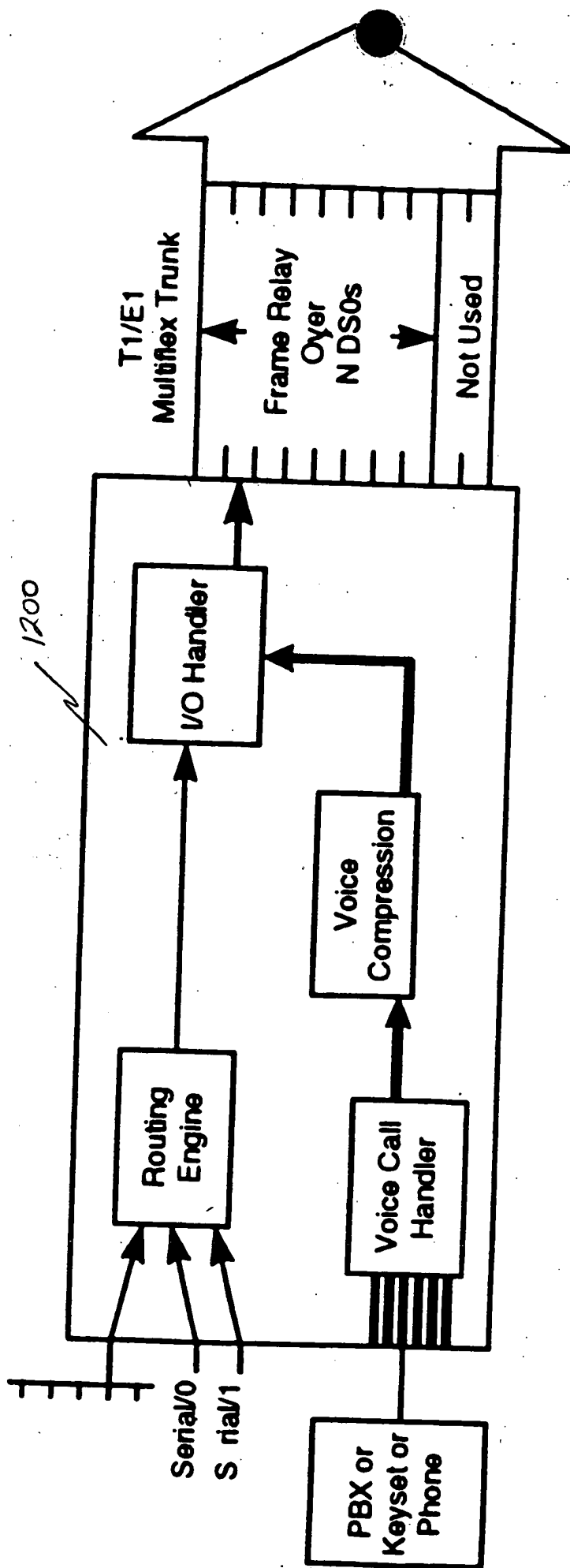


FIGURE 12

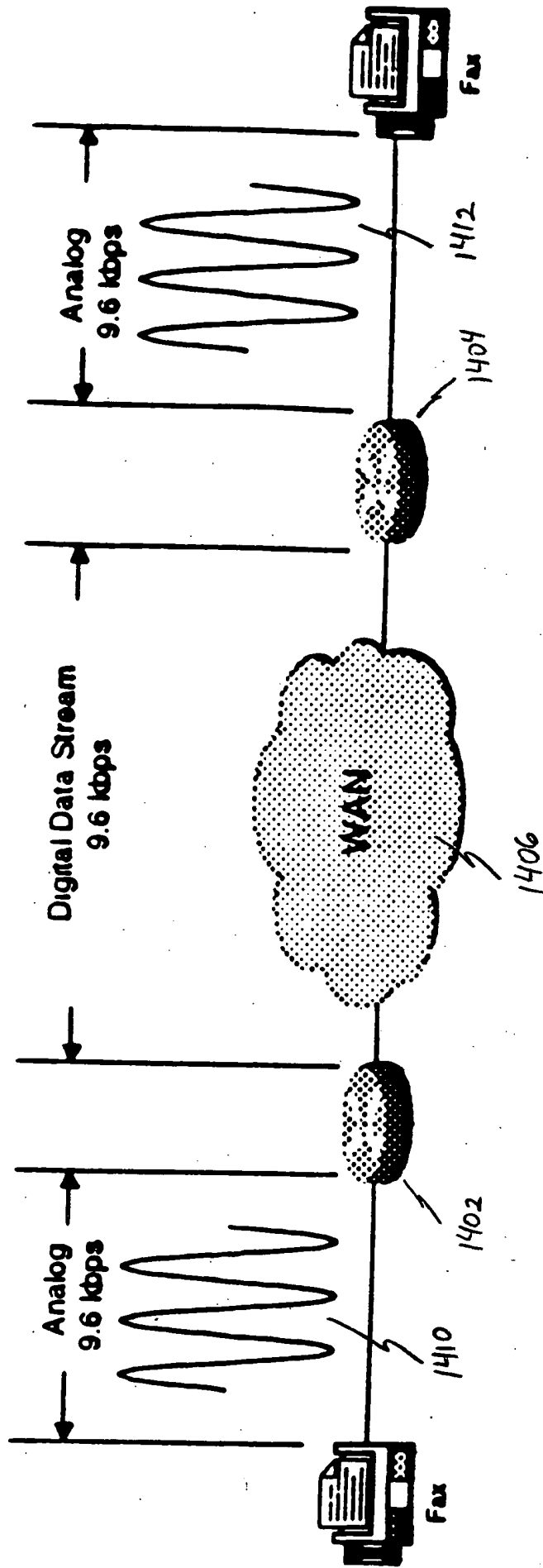


FIGURE 14

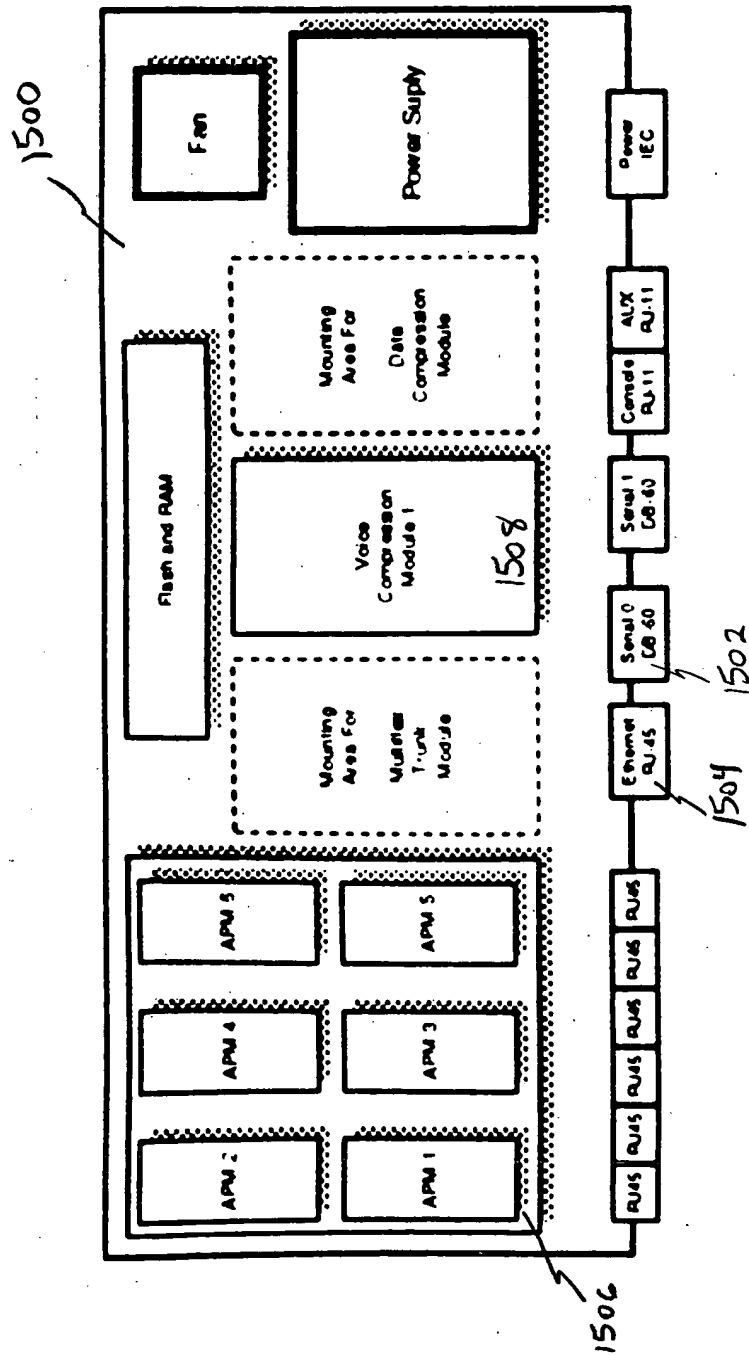


FIGURE 15

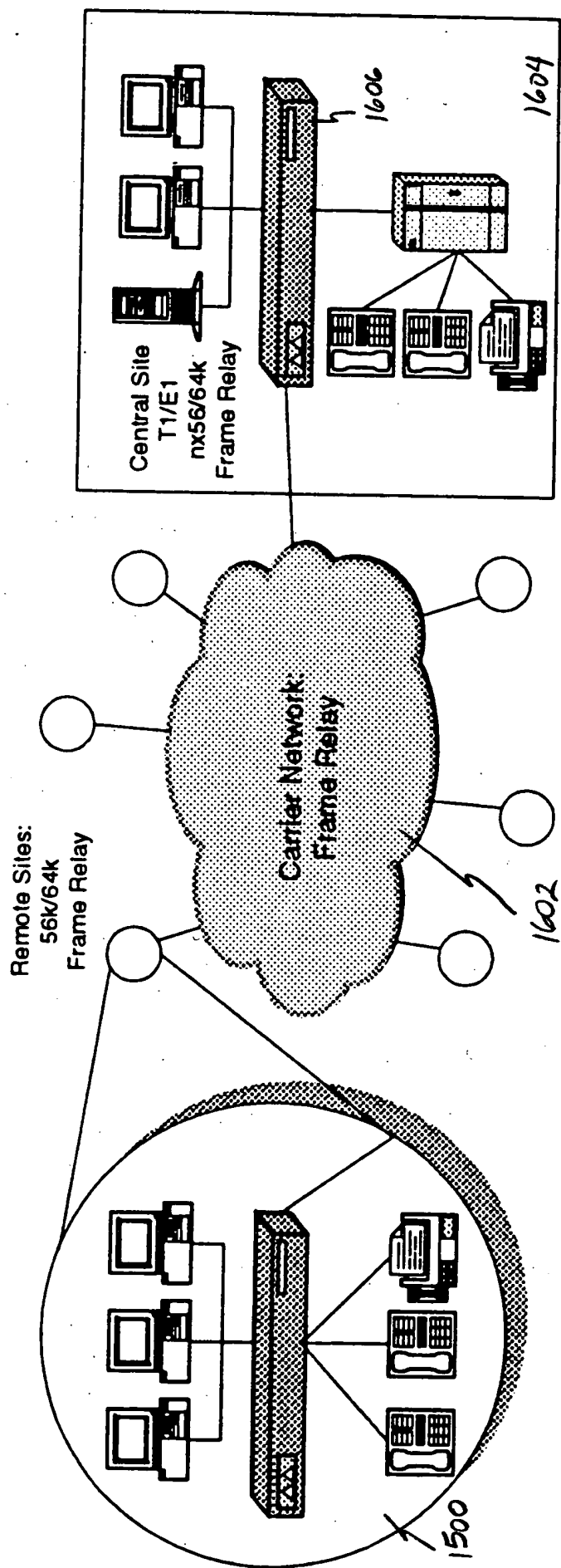


FIGURE 16

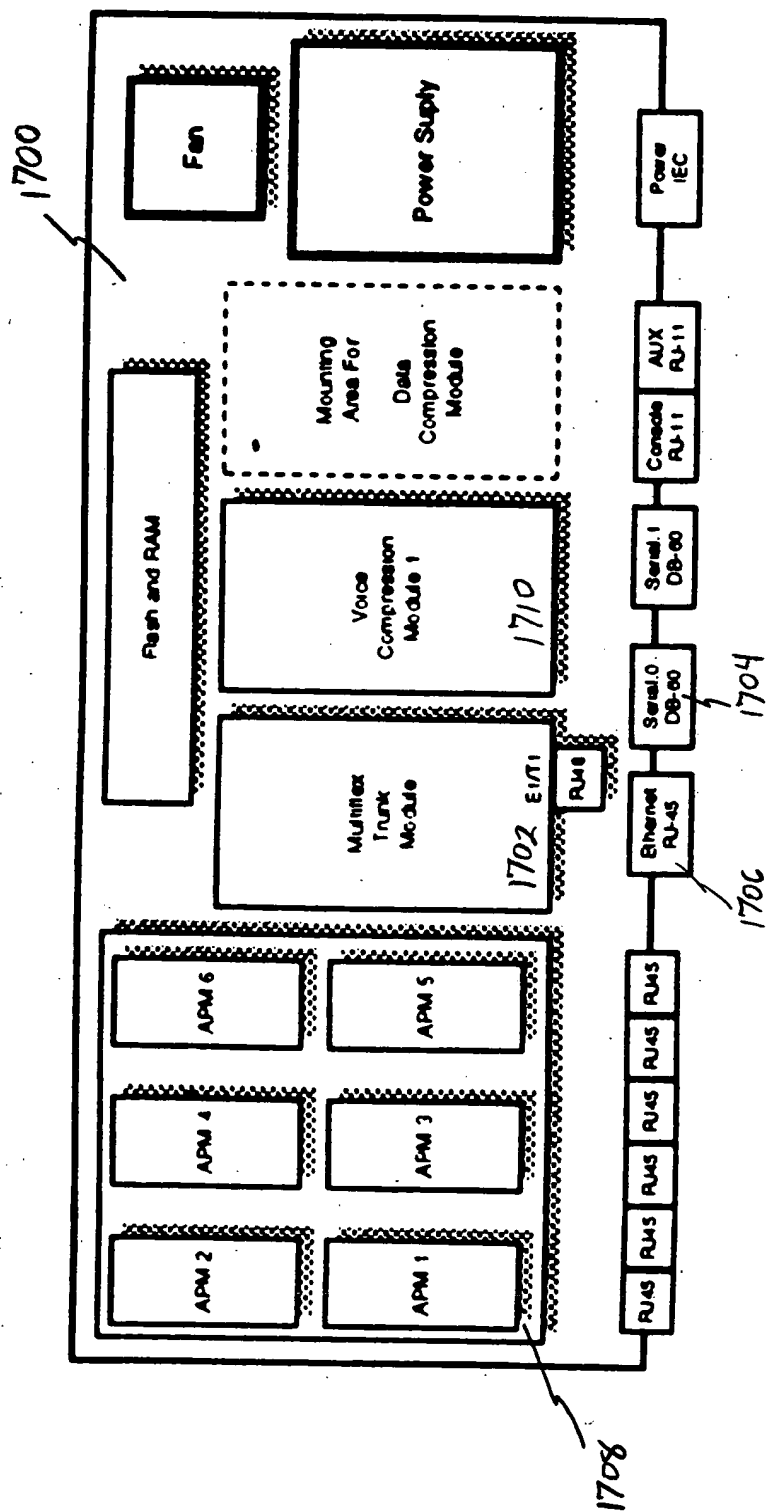


FIGURE 17

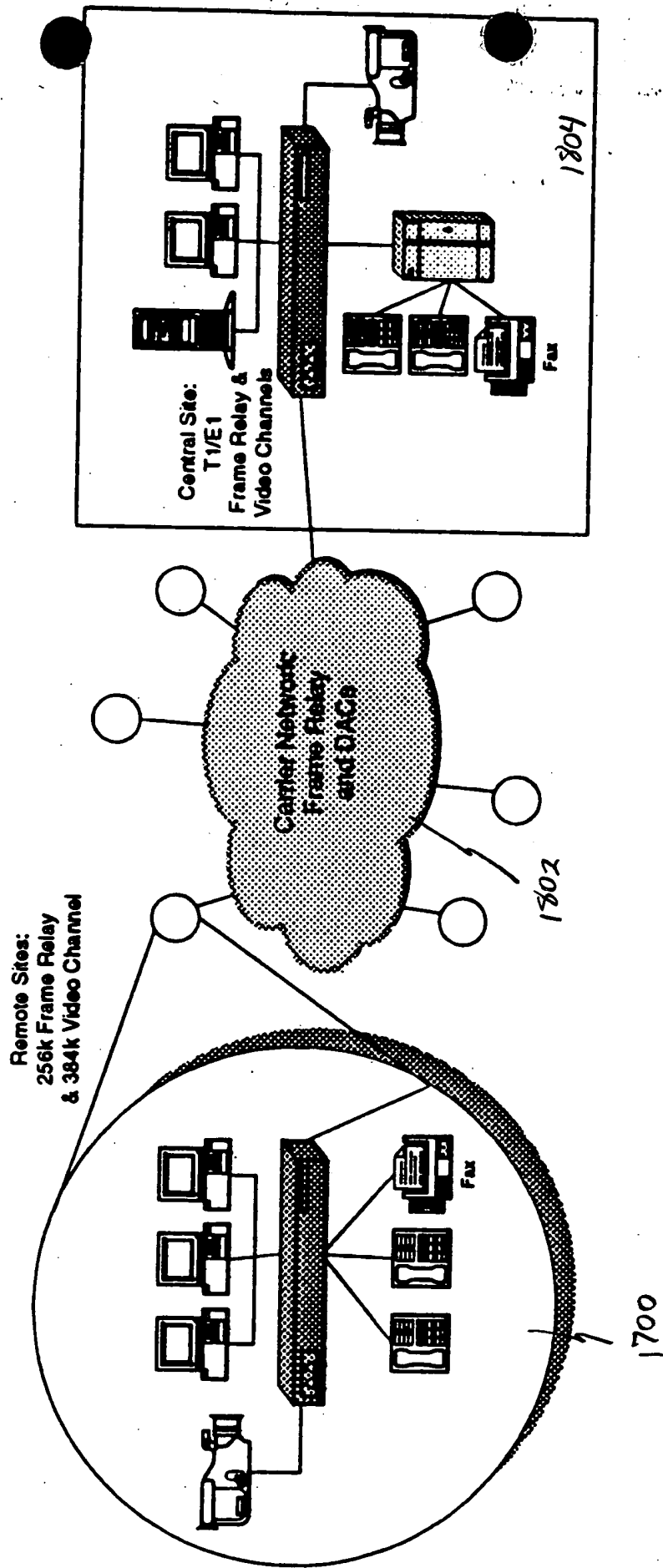


Figure 18

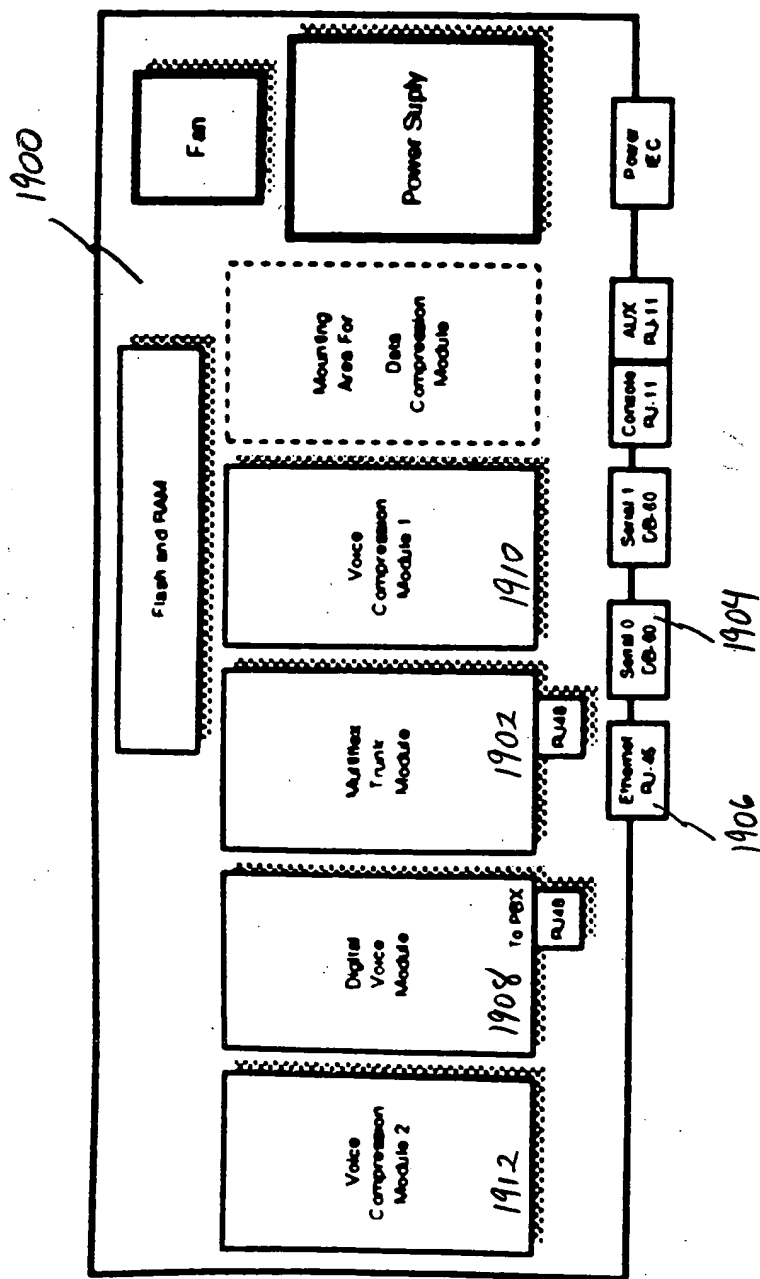


FIGURE 19

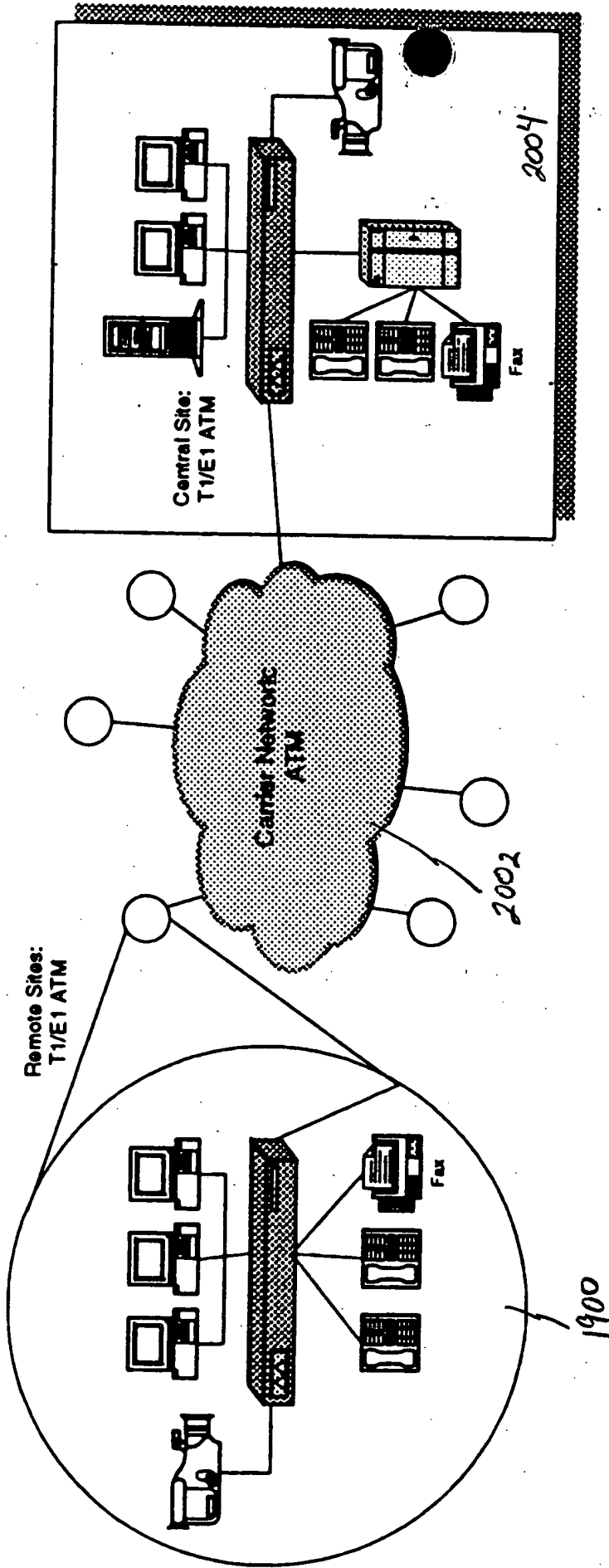


FIGURE 20

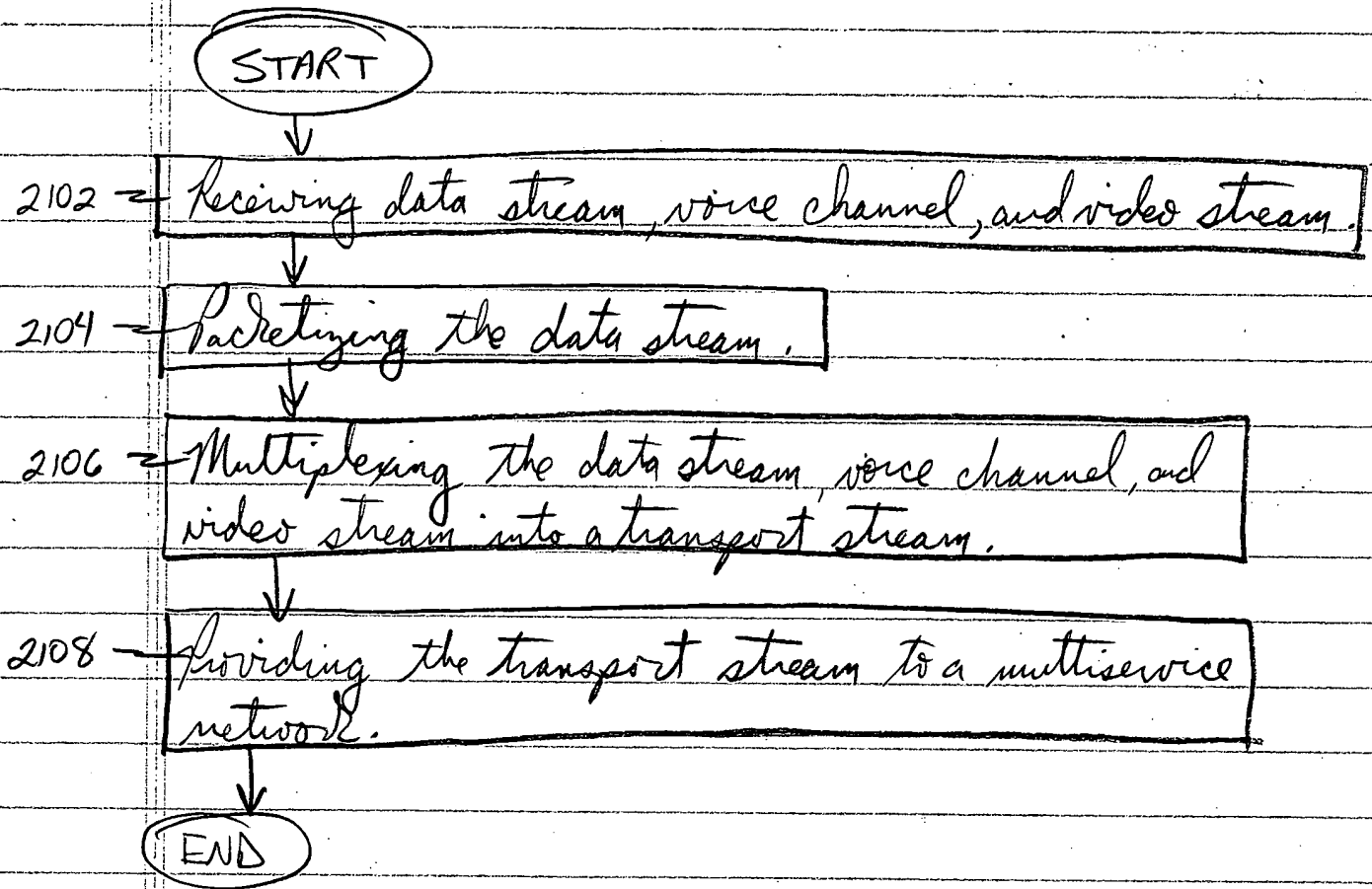


FIGURE 21

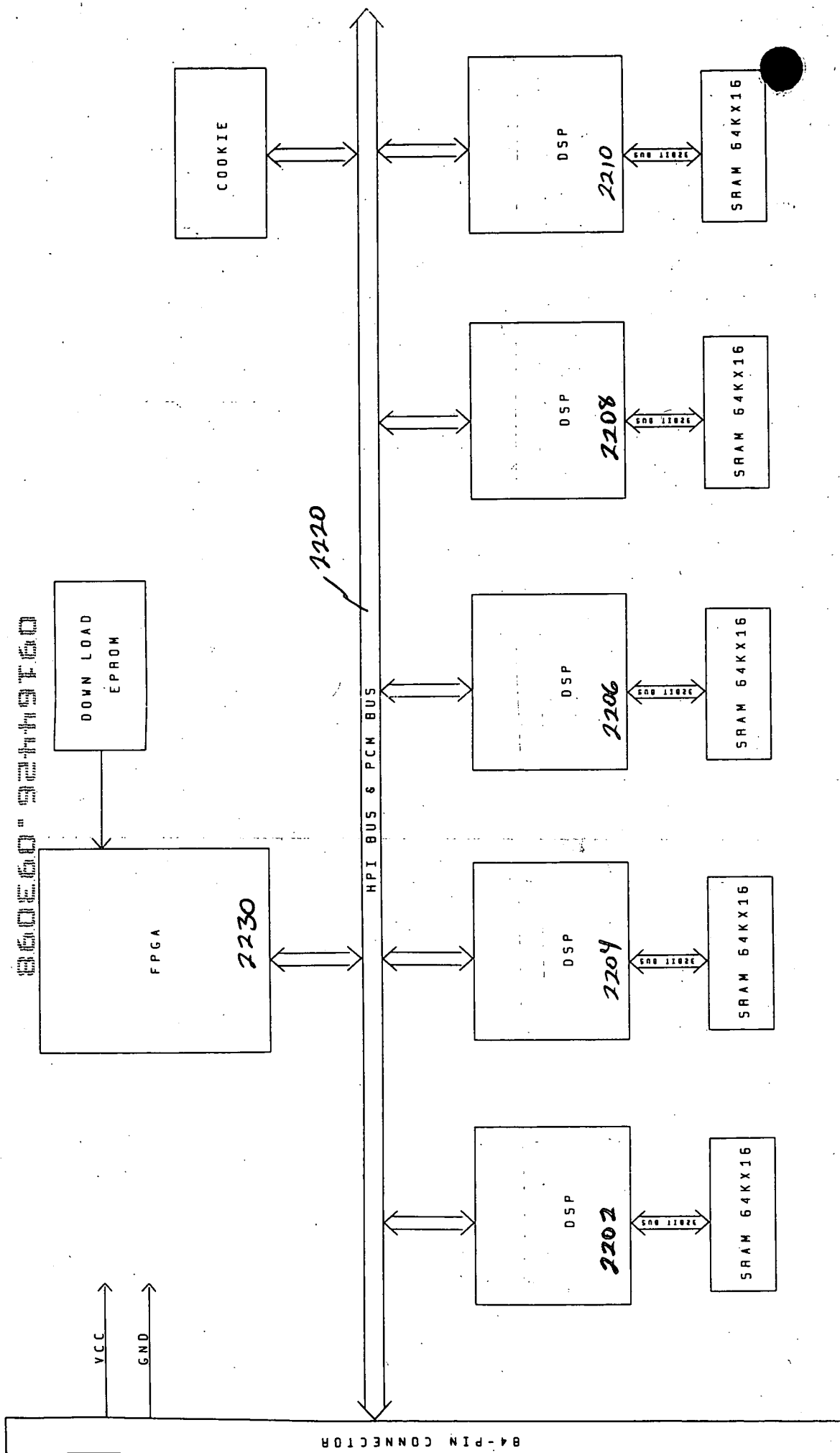


FIGURE 22

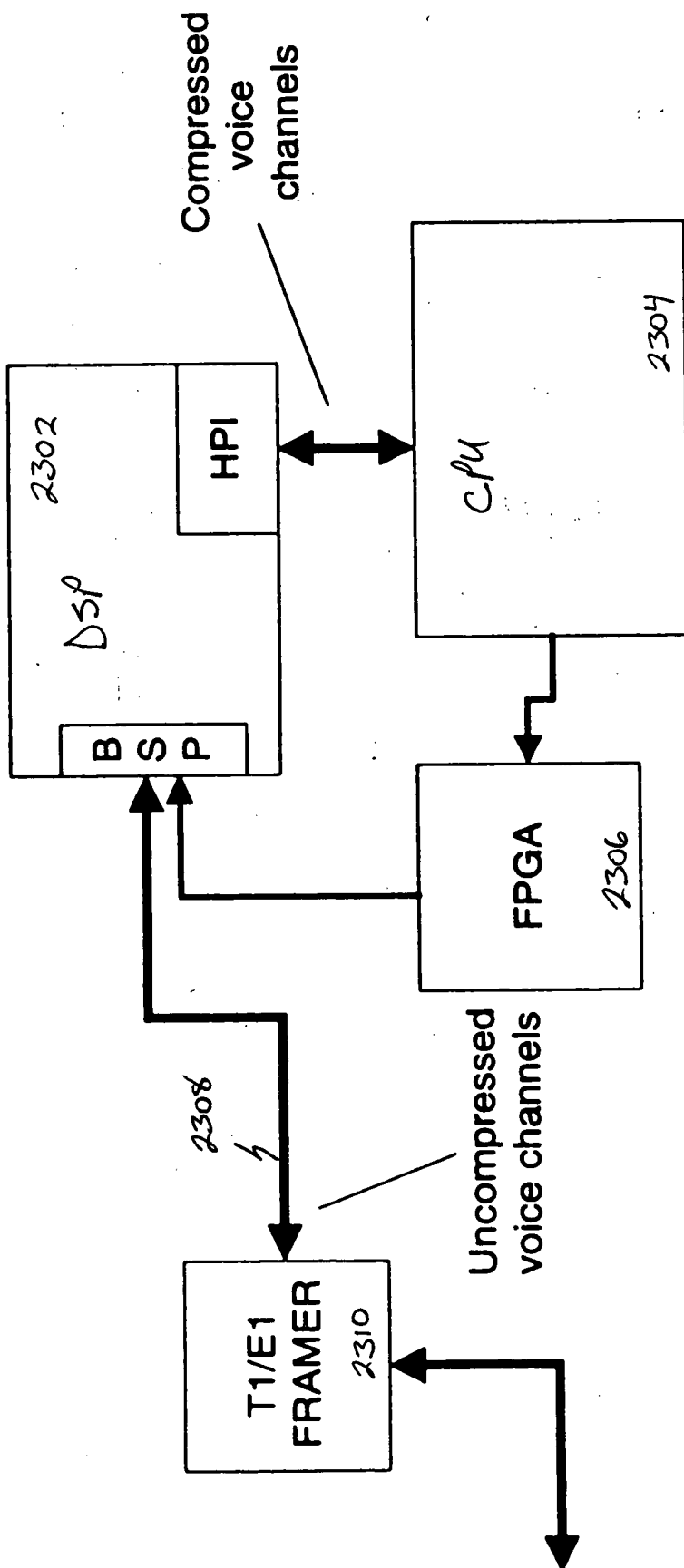


FIGURE 23

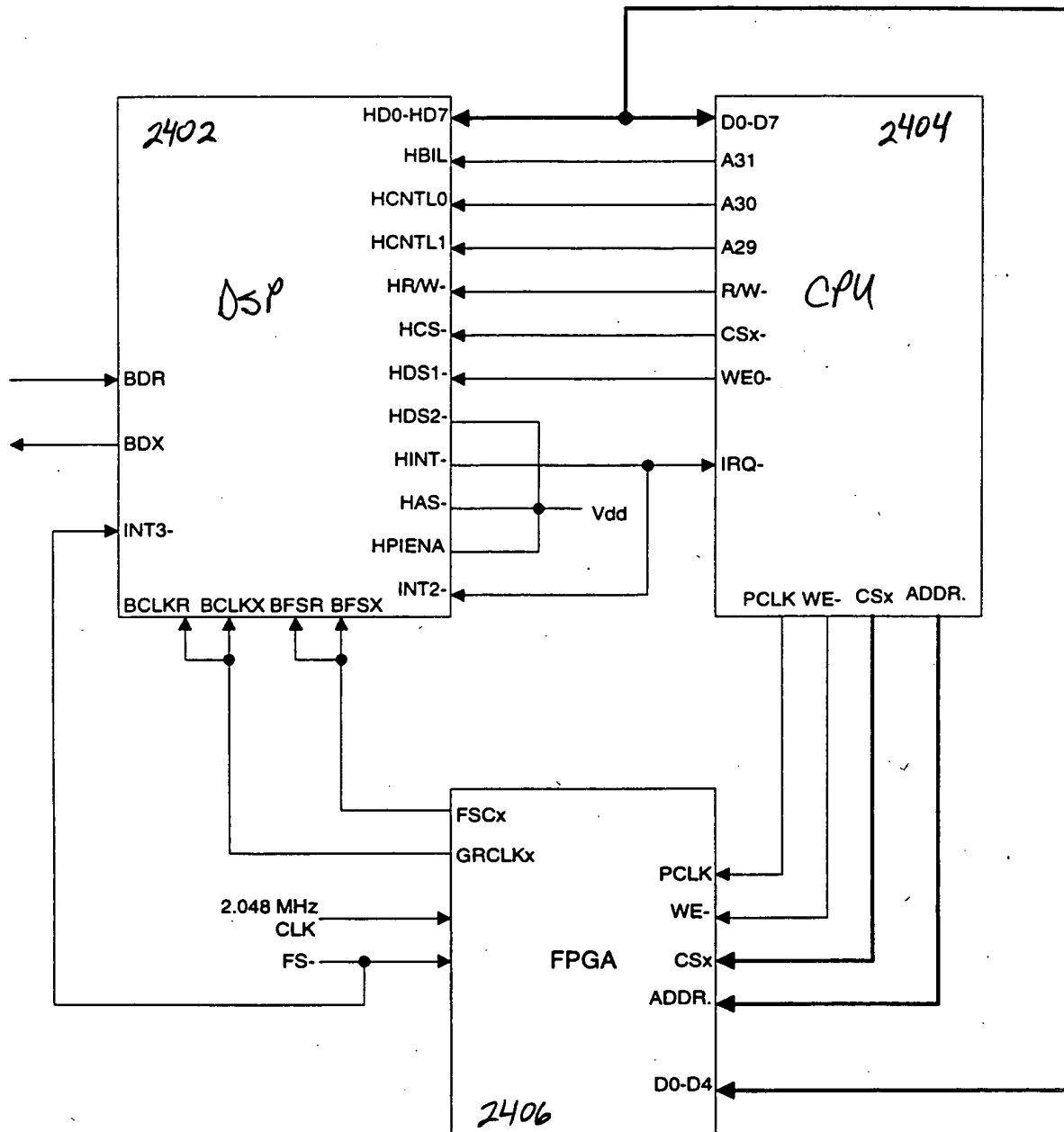


FIGURE 24

360E60-9249T60

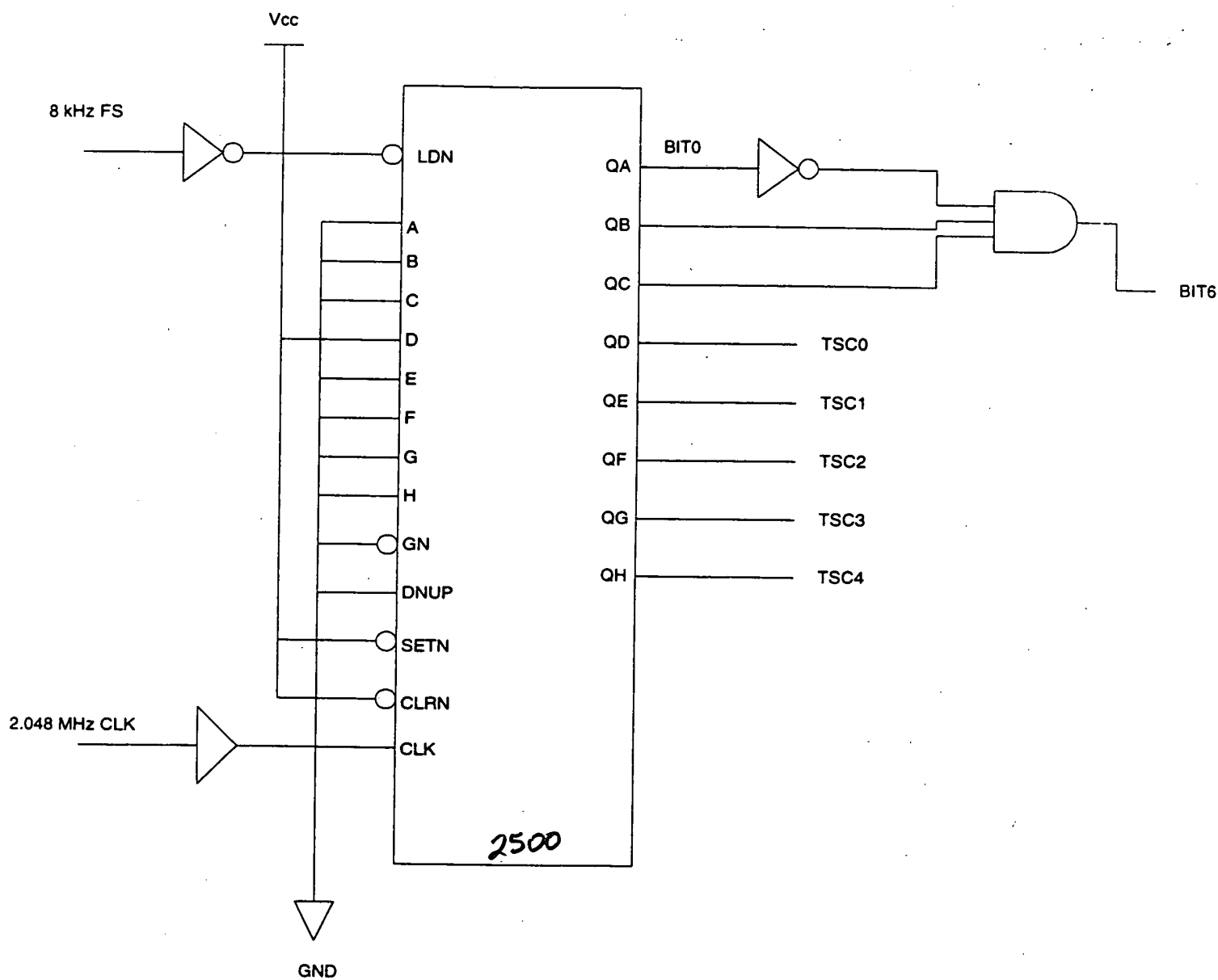


FIGURE 25

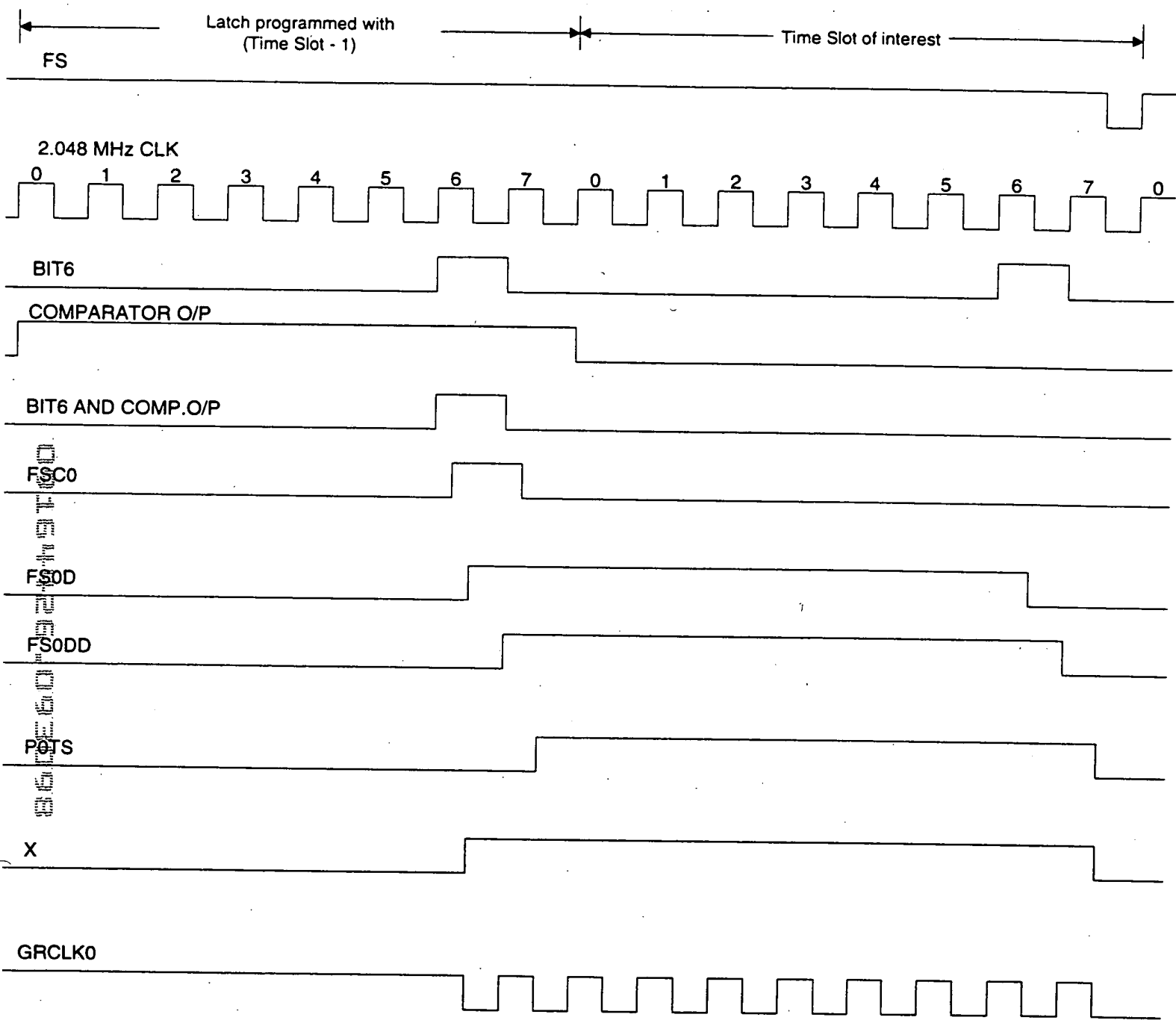


FIGURE 26

091544-9249T60

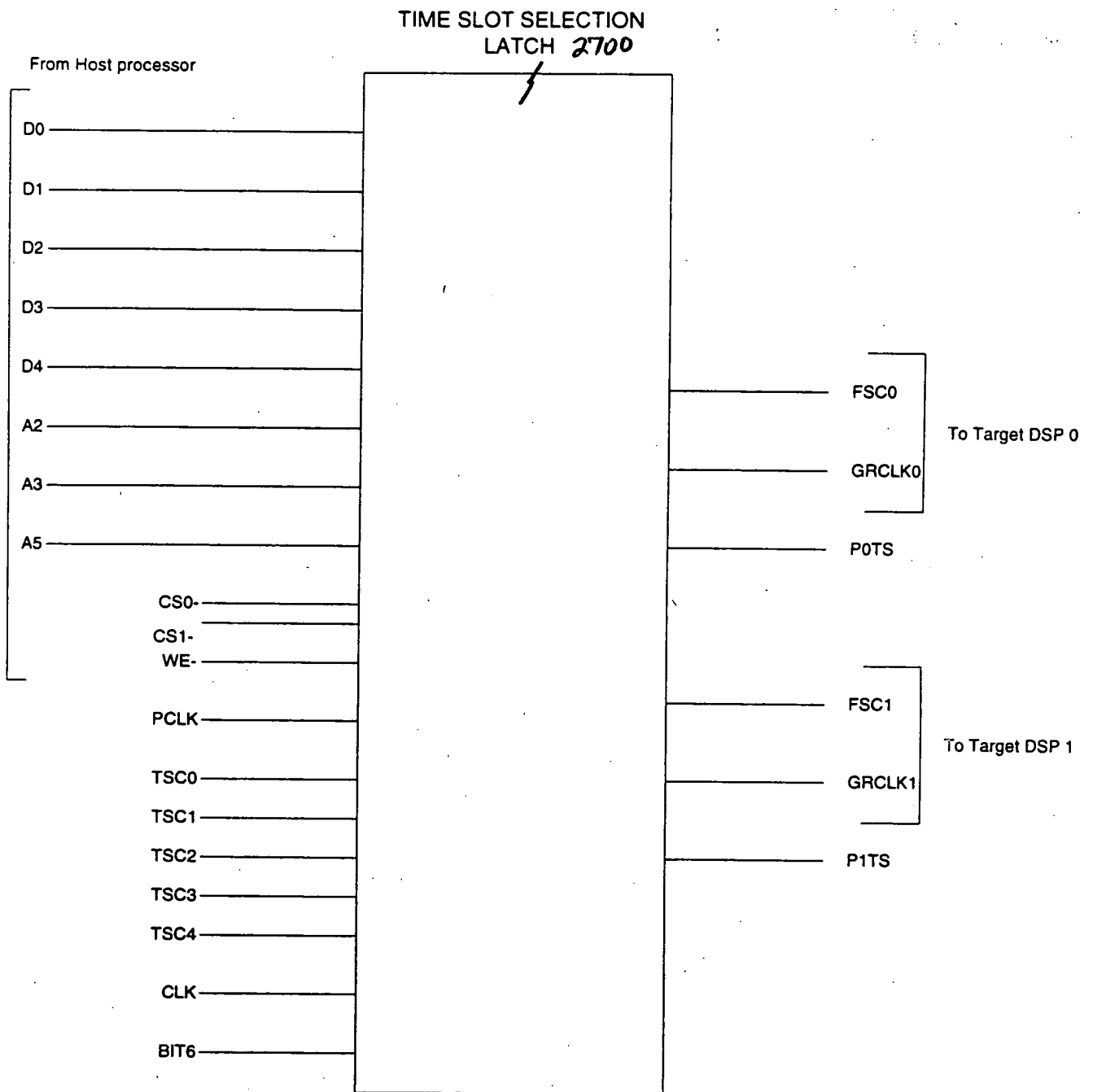
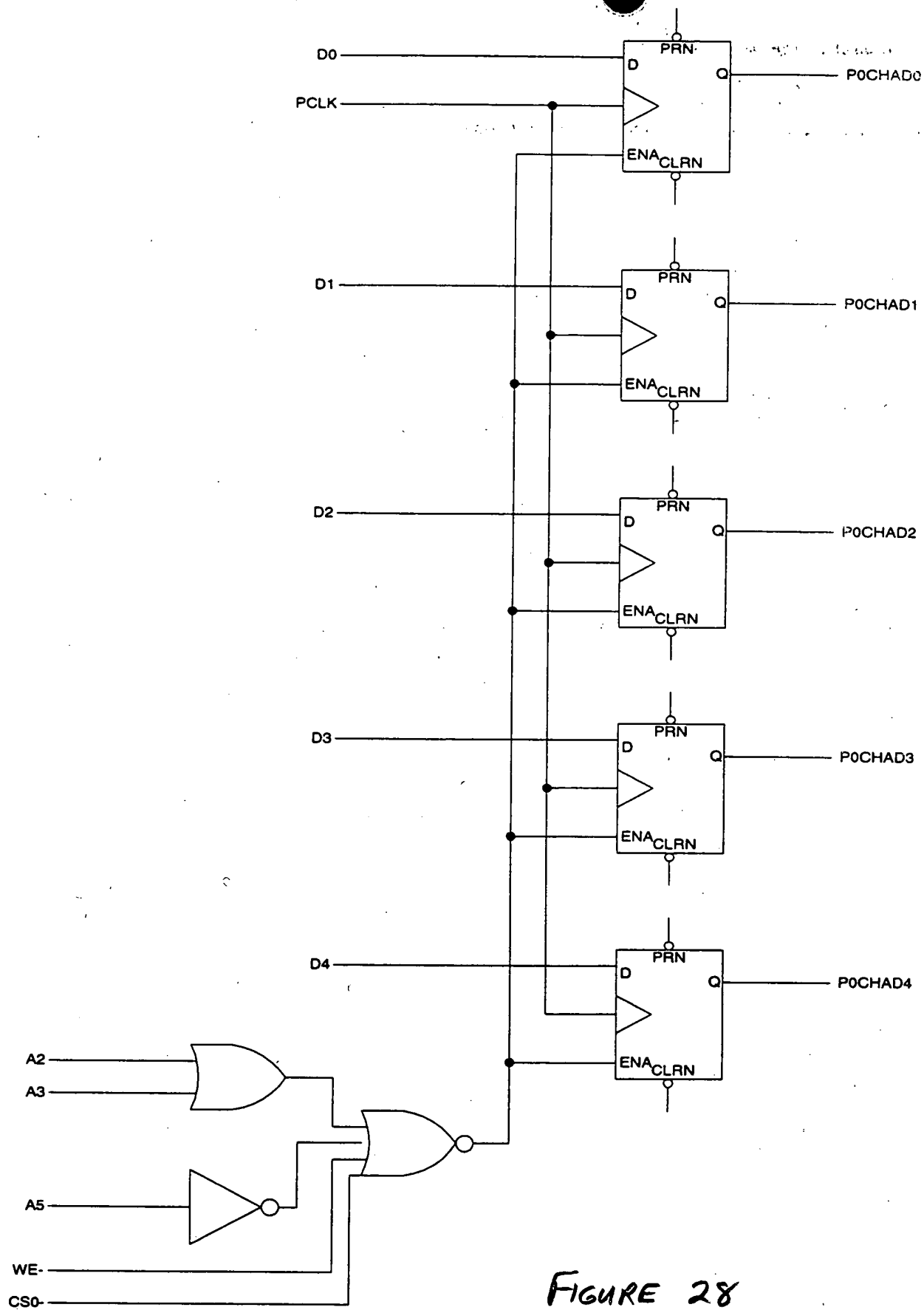


FIGURE 27



860E60" 92479T60

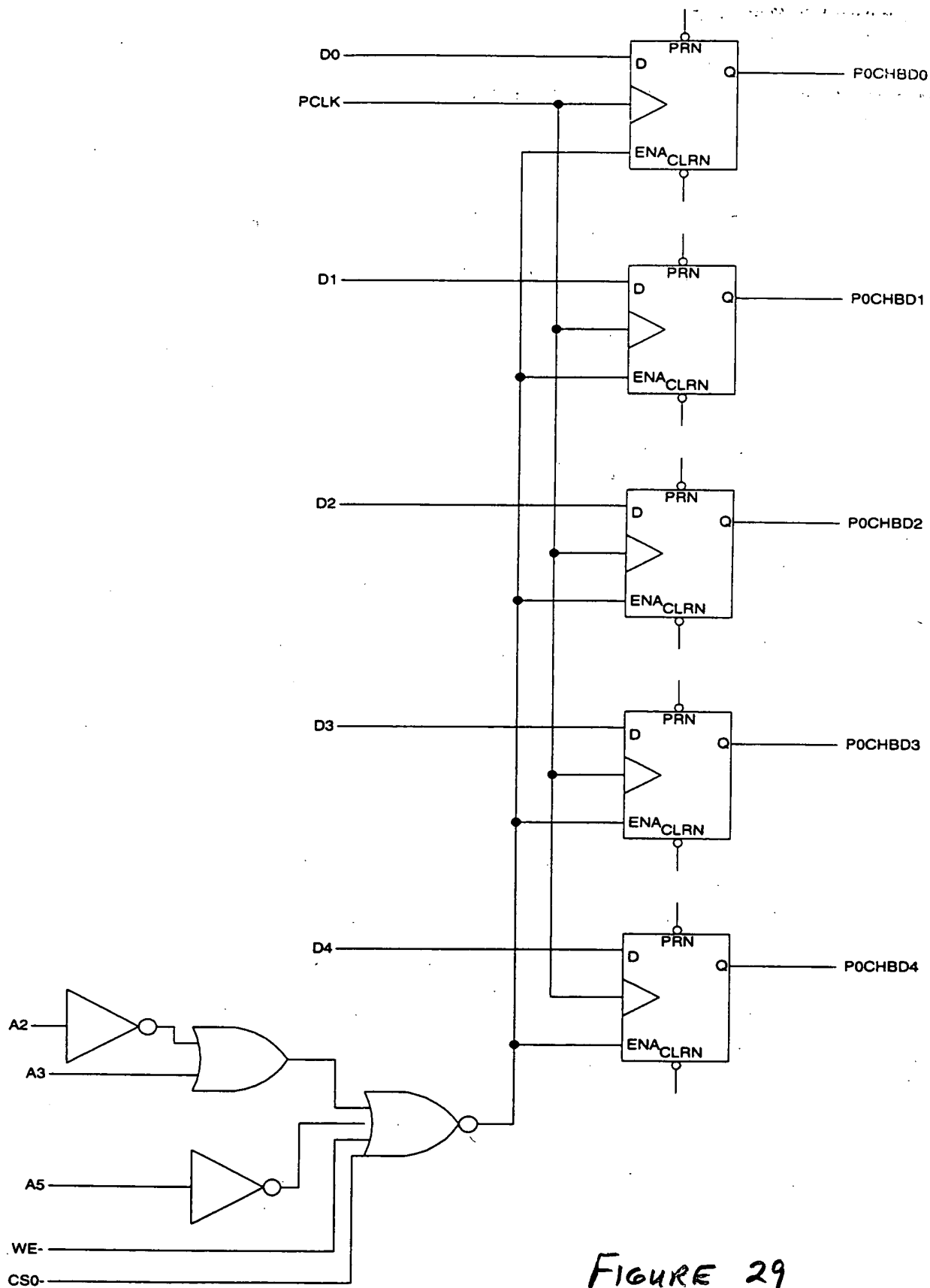


FIGURE 29

The diagram shows a logic circuit for a 3002 decoder. It has 10 inputs: P0CHAD0, TSC0, P0CHAD1, TSC1, P0CHAD2, TSC2, P0CHAD3, TSC3, P0CHAD4, TSC4, P0CHBD0, TSC0, P0CHBD1, TSC1, P0CHBD2, TSC2, P0CHBD3, TSC3, P0CHBD4, and TSC4. The circuit uses 10 XOR gates to generate 10 intermediate signals. These are then combined using a series of AND gates (labeled 3004 and 3006) to produce 16 outputs: FS0, FSC0, CLK, BIT6, and TSE0-. The circuit is labeled 3002 at the bottom.

FIGURE 30

860E50-92479F60

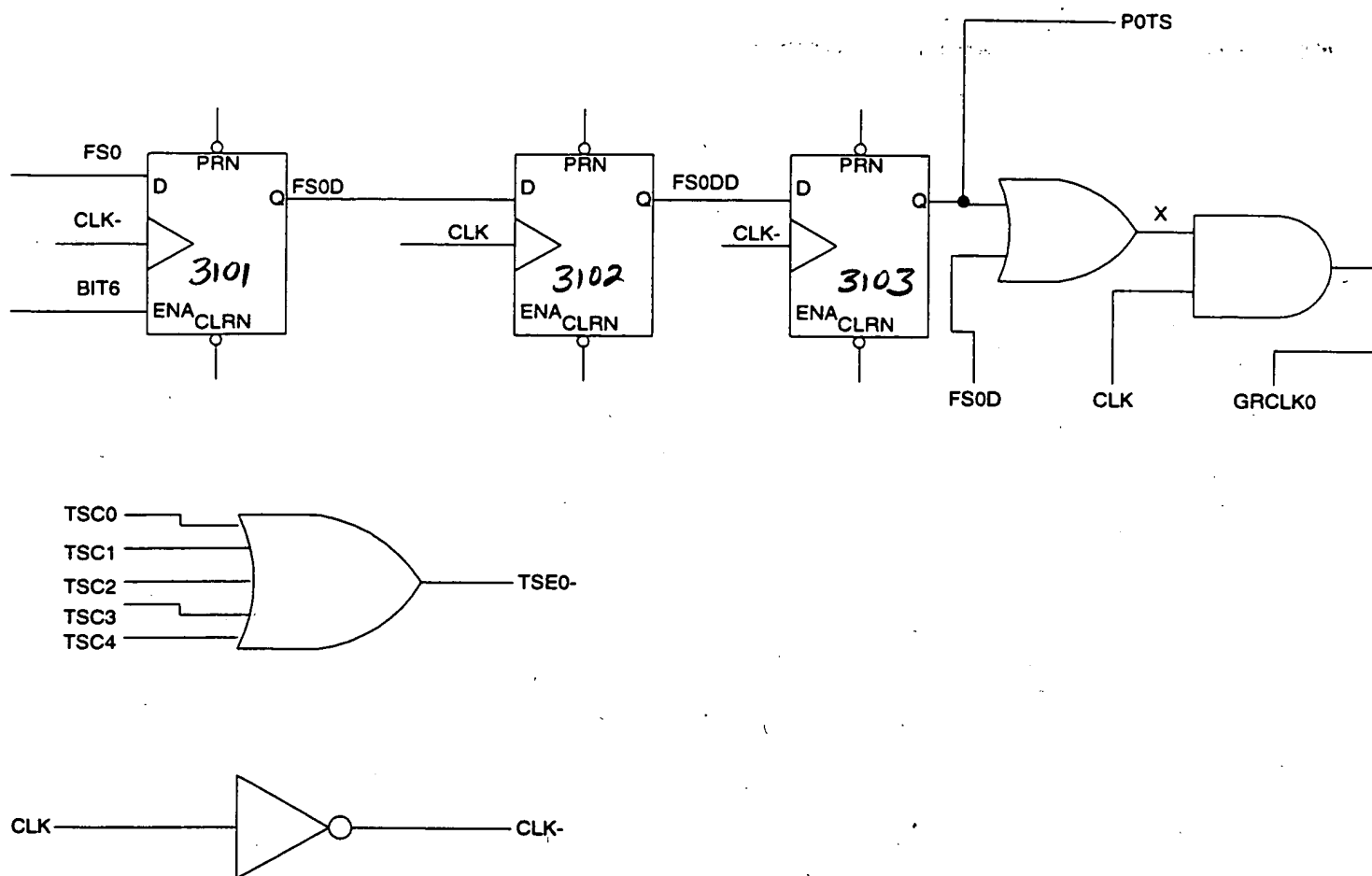


FIGURE 31

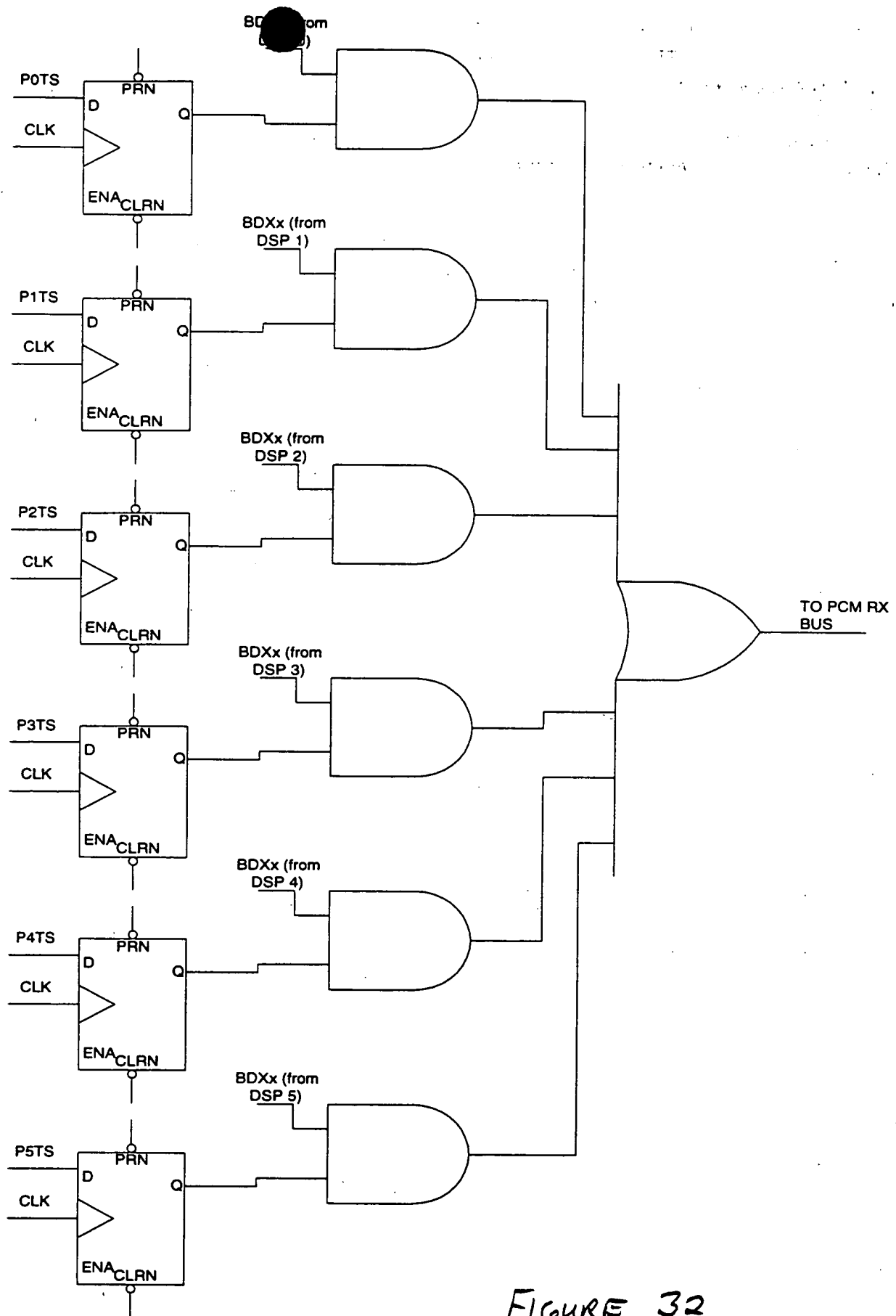


FIGURE 32

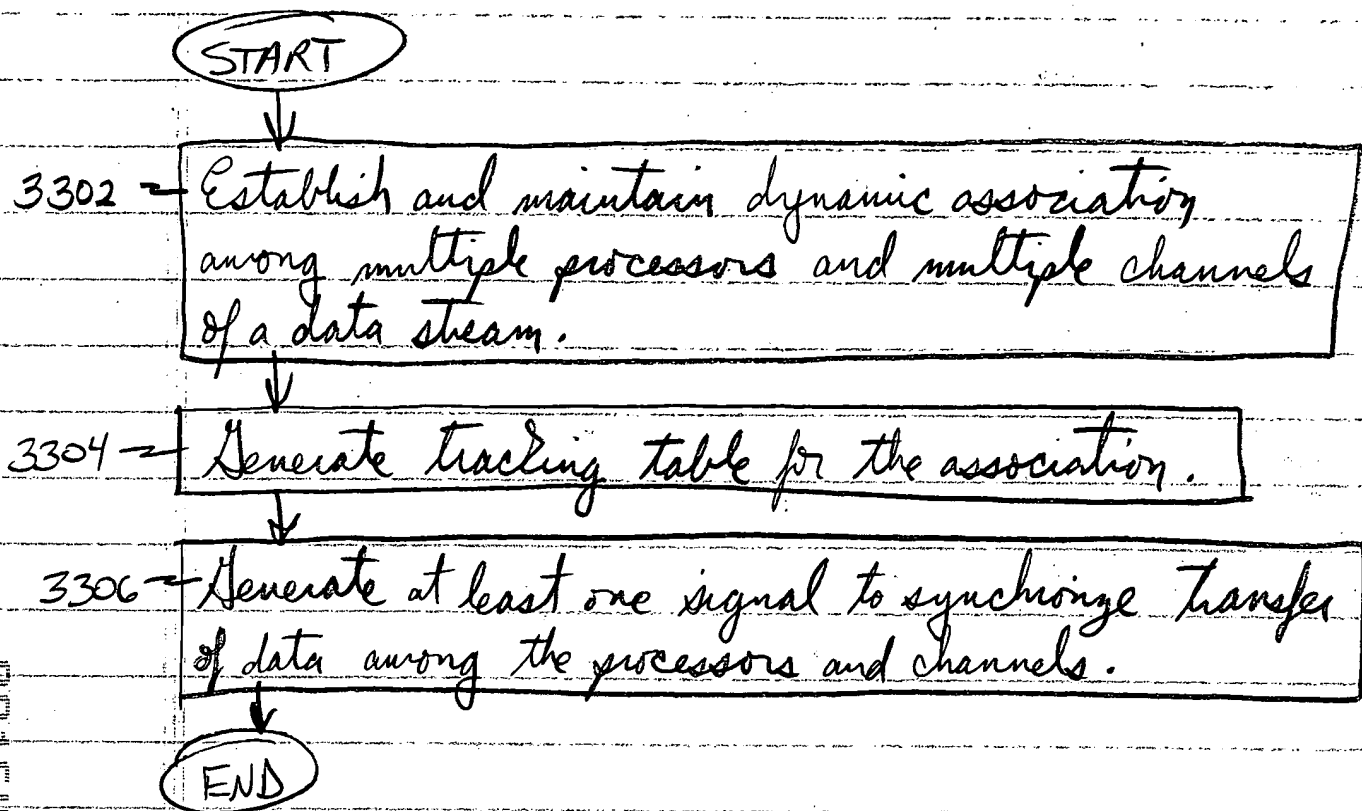


FIGURE 33

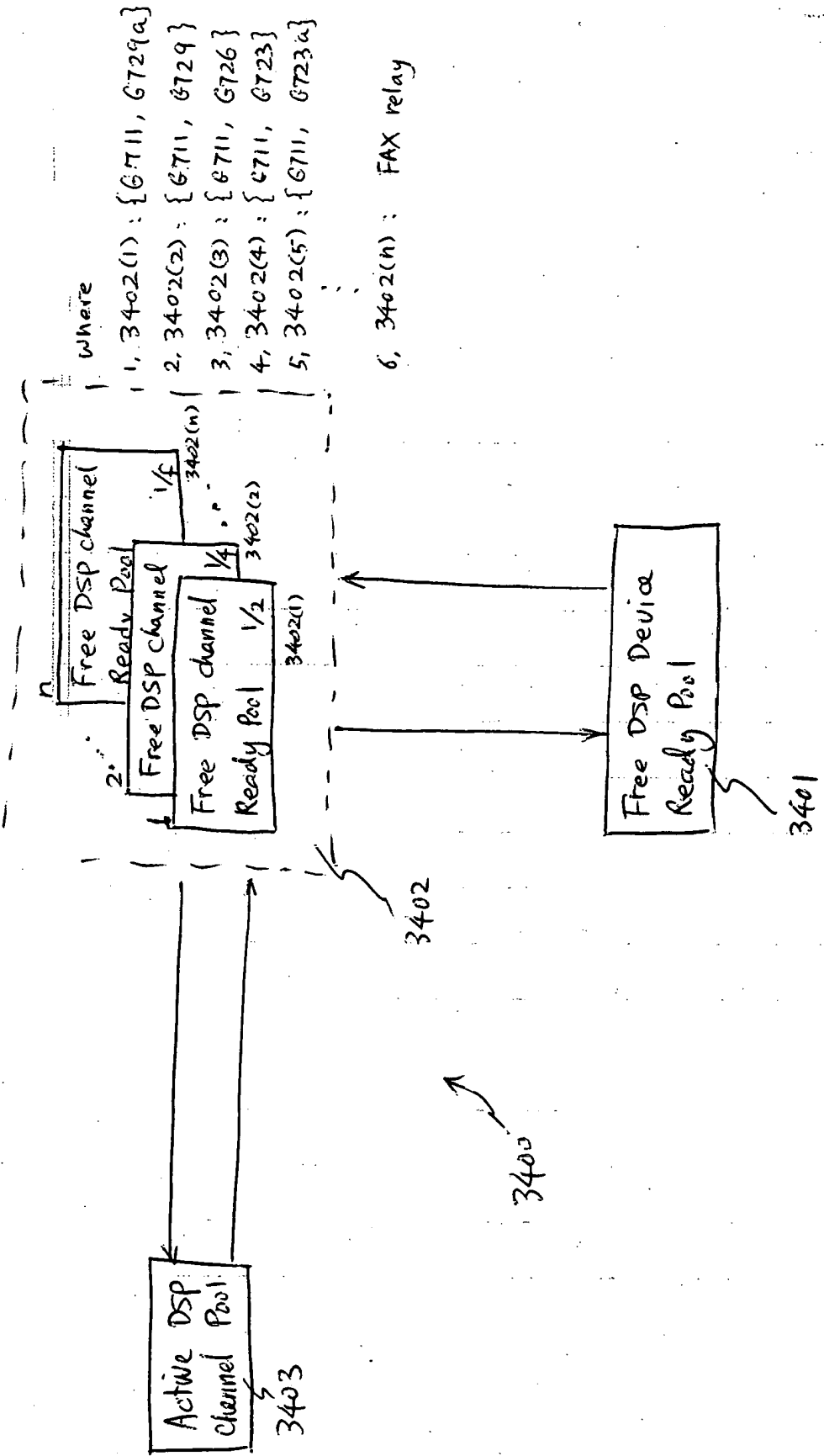


Figure 34

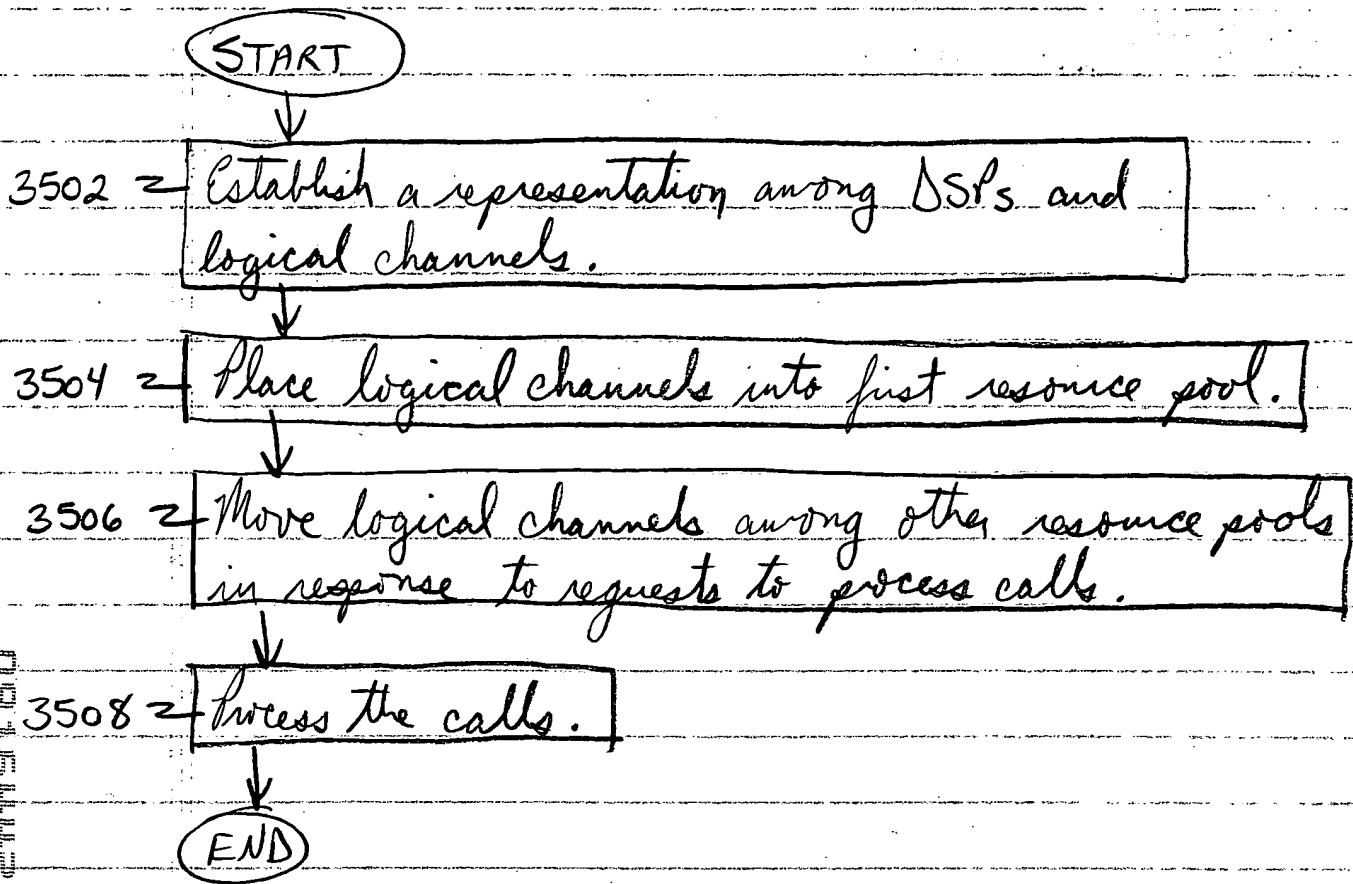


FIGURE 35

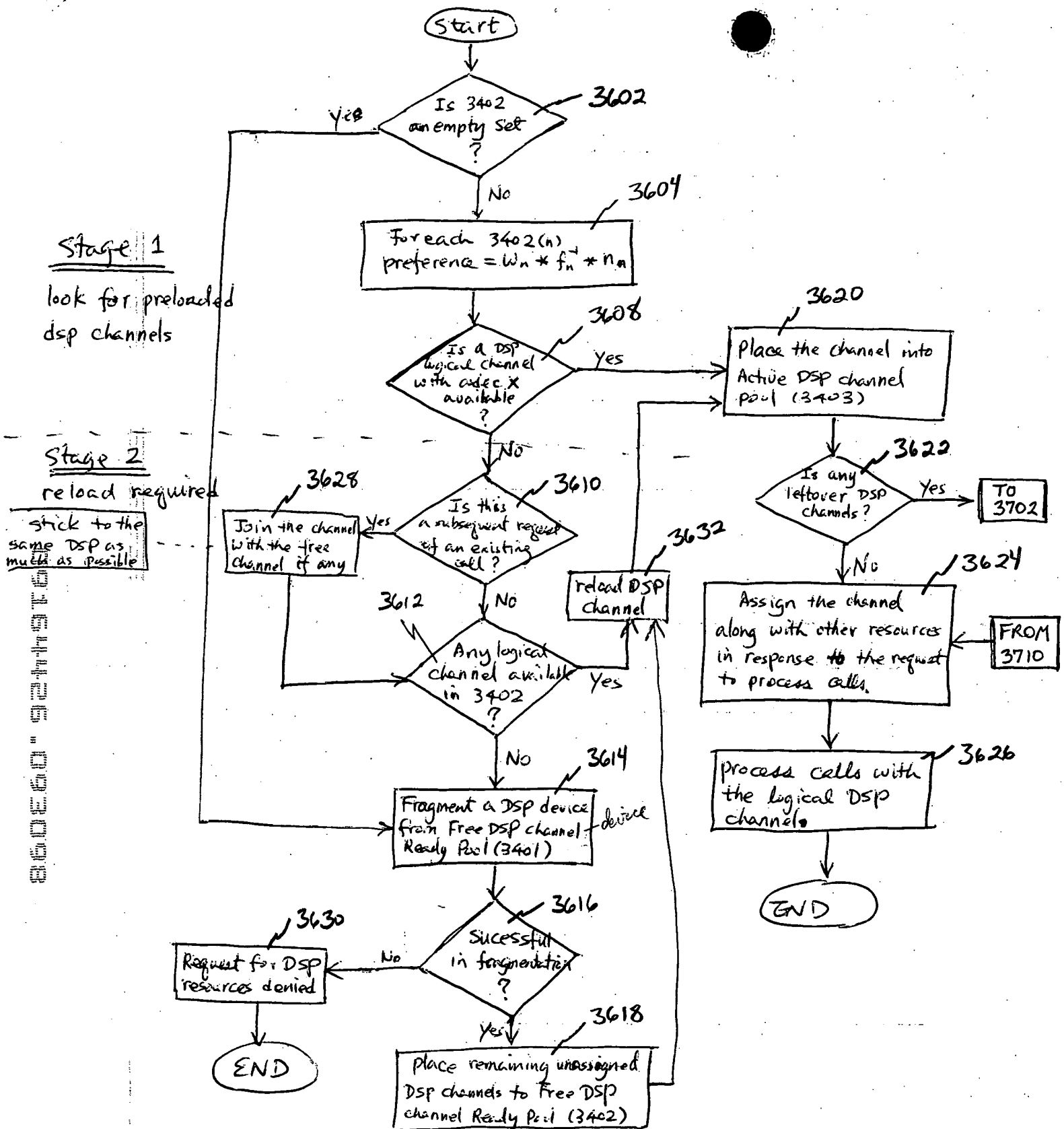


FIGURE 36

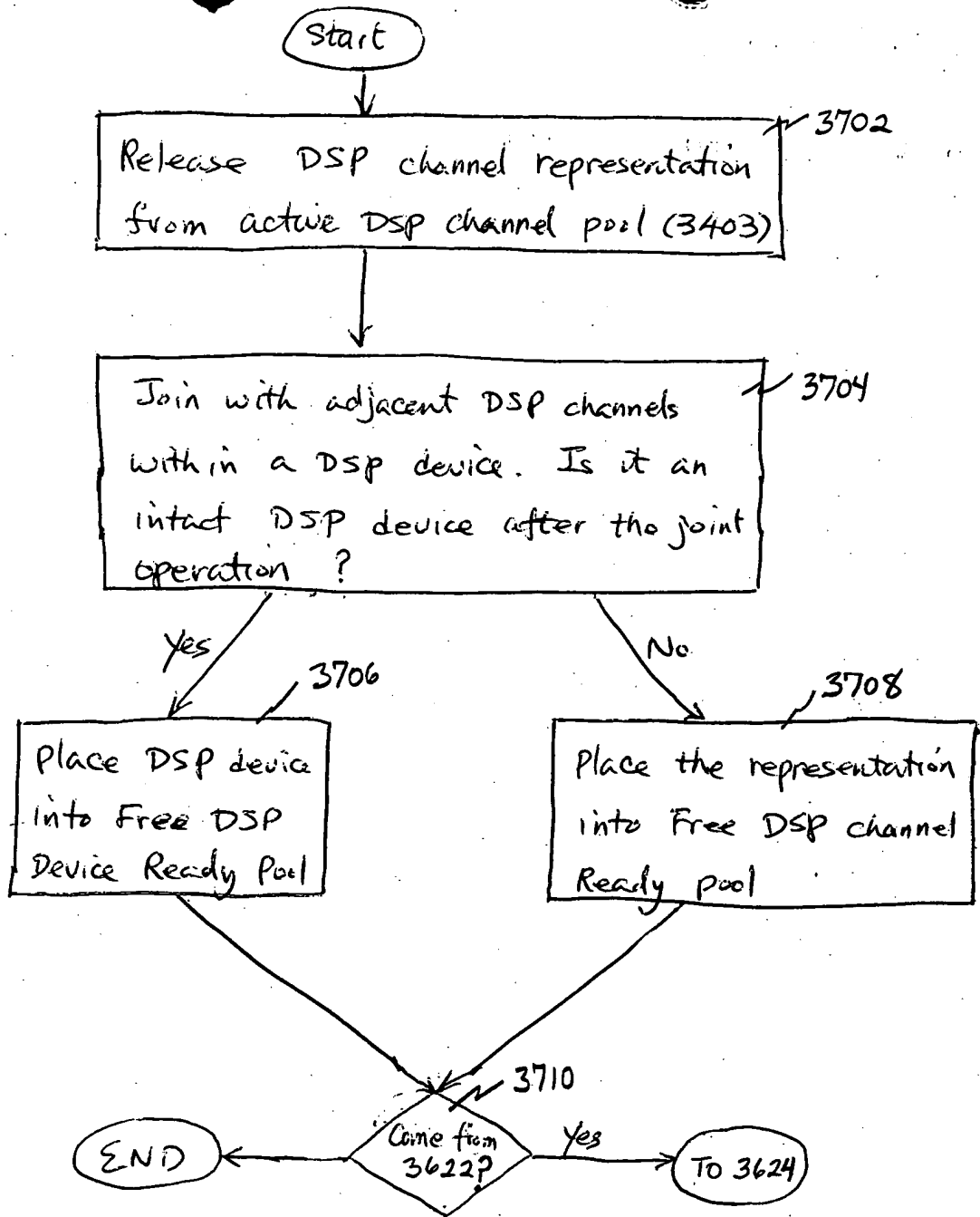


FIGURE 37

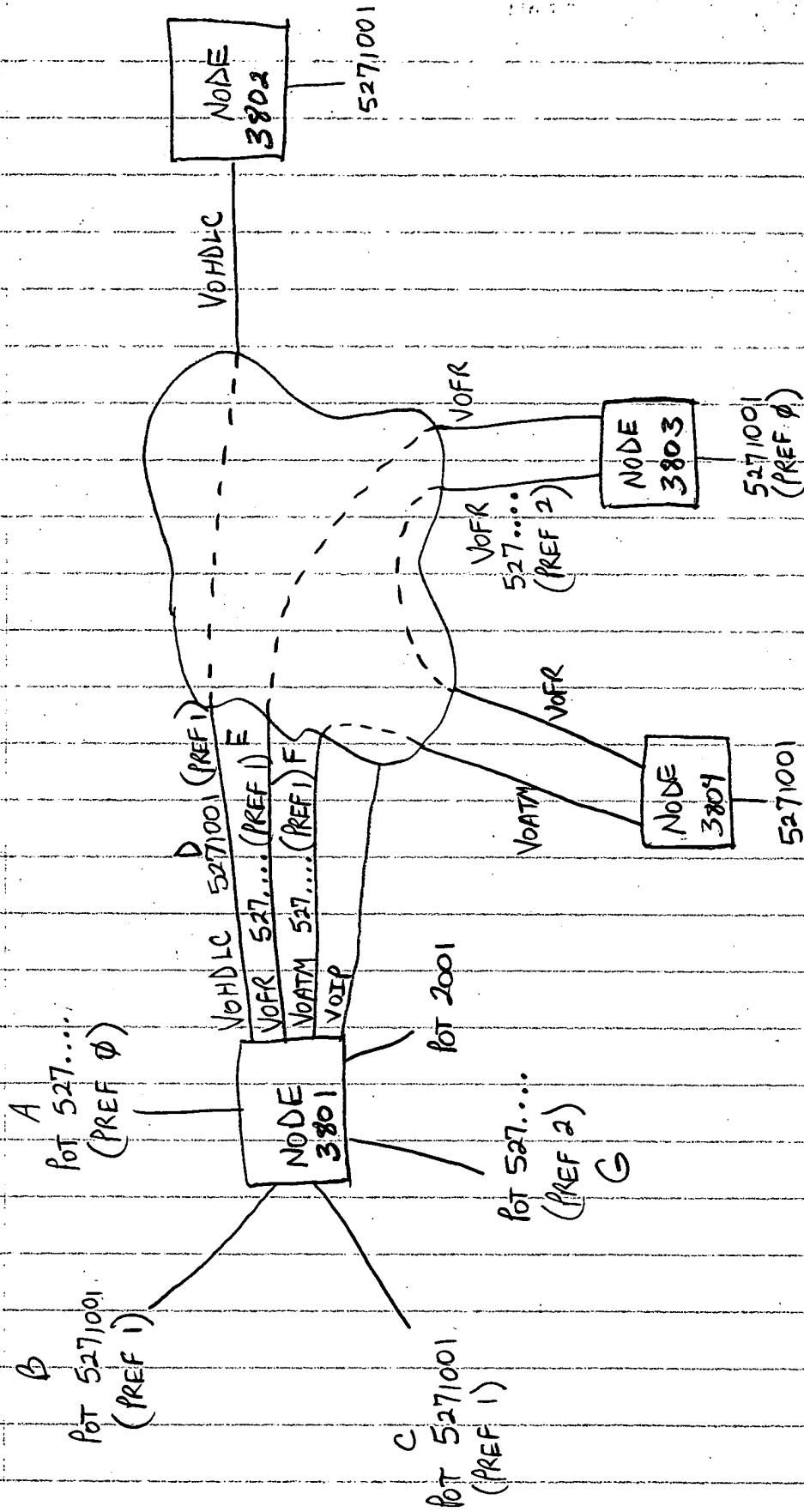


Figure 38

PRIORITY

1	POT 527.... (PREF 0)	A
2	POT 527 1001 (PREF 1)	B
3	POT 527 1001 (PREF 1)	C
4	VOHDL 527 1001 (PREF 1)	D
5	VOFR 527.... (PREF 1)	E
6	VOATM 527.... (PREF 1)	F
7	POT 527.... (PREF 2)	G

FIGURE 39

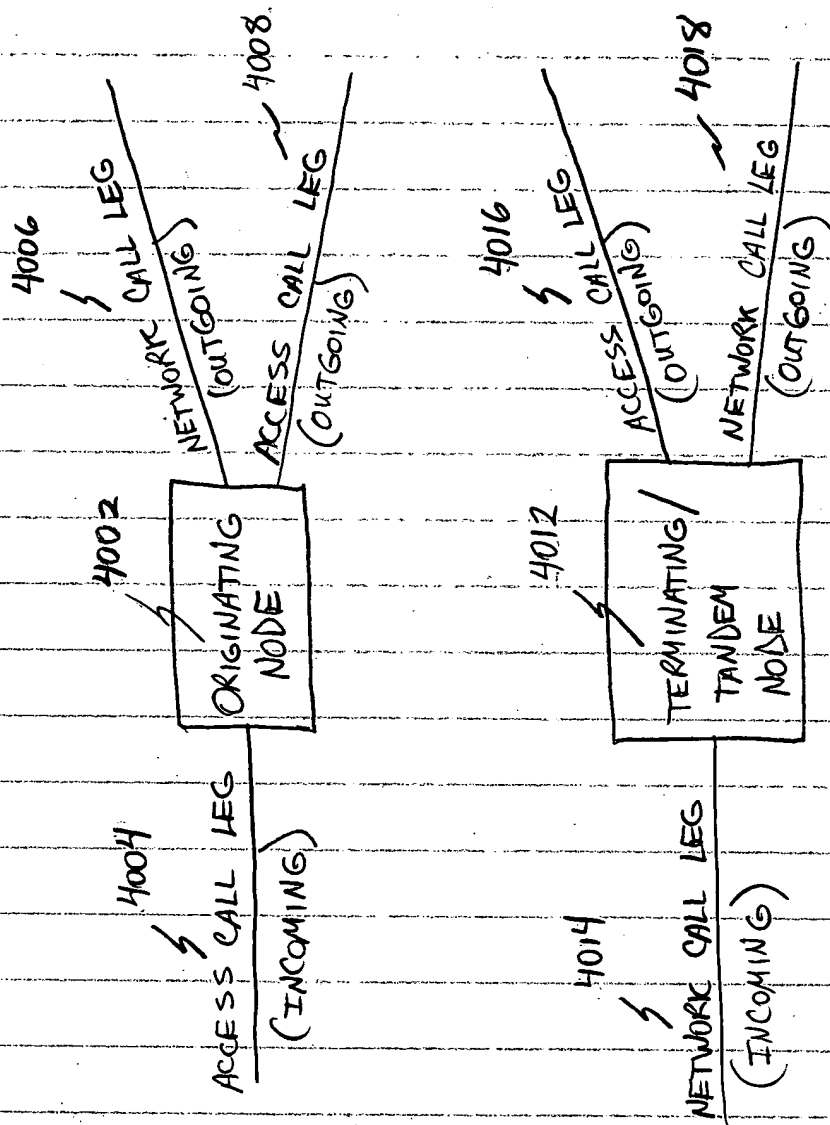


FIGURE 40

860E60 9249F60

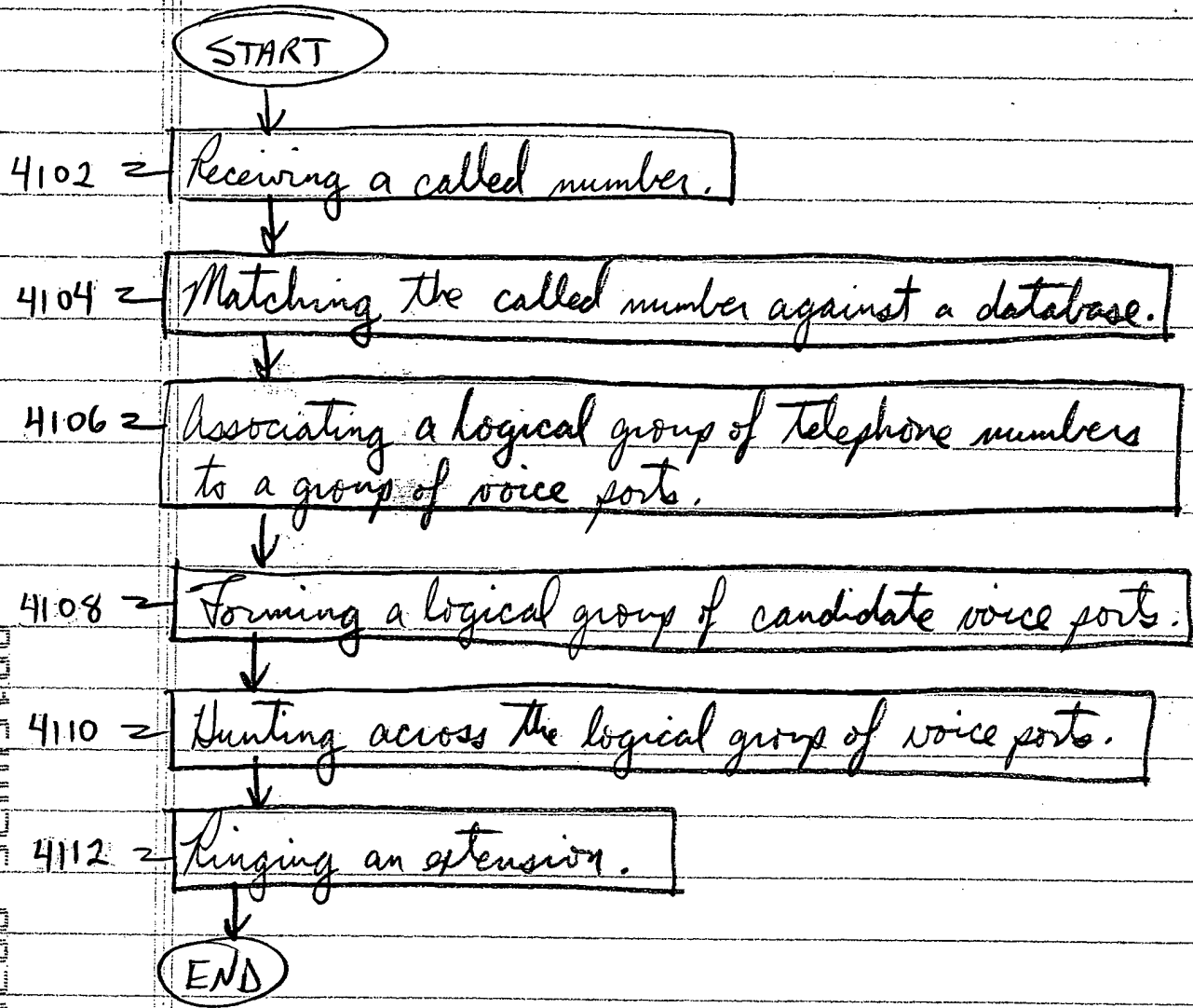


FIGURE 41

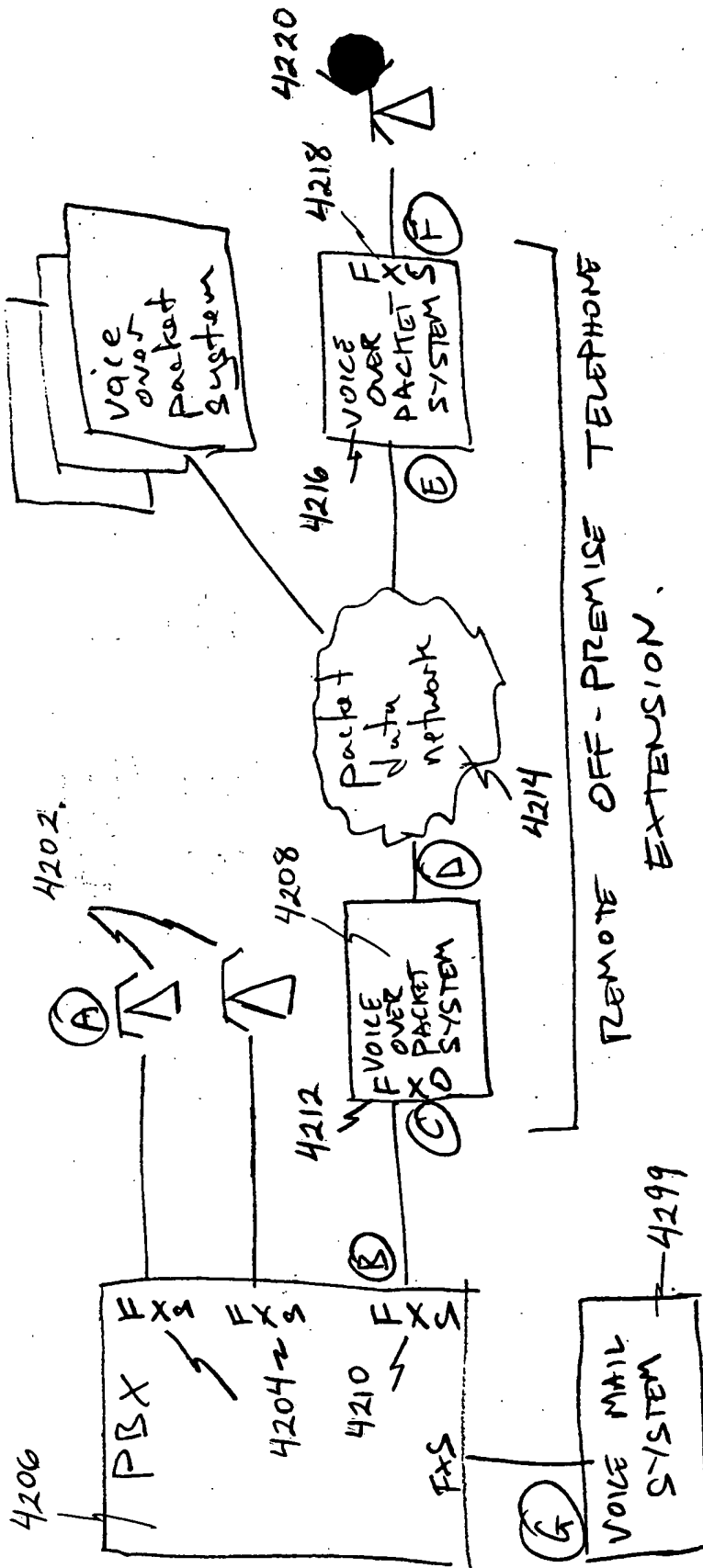


FIGURE 42

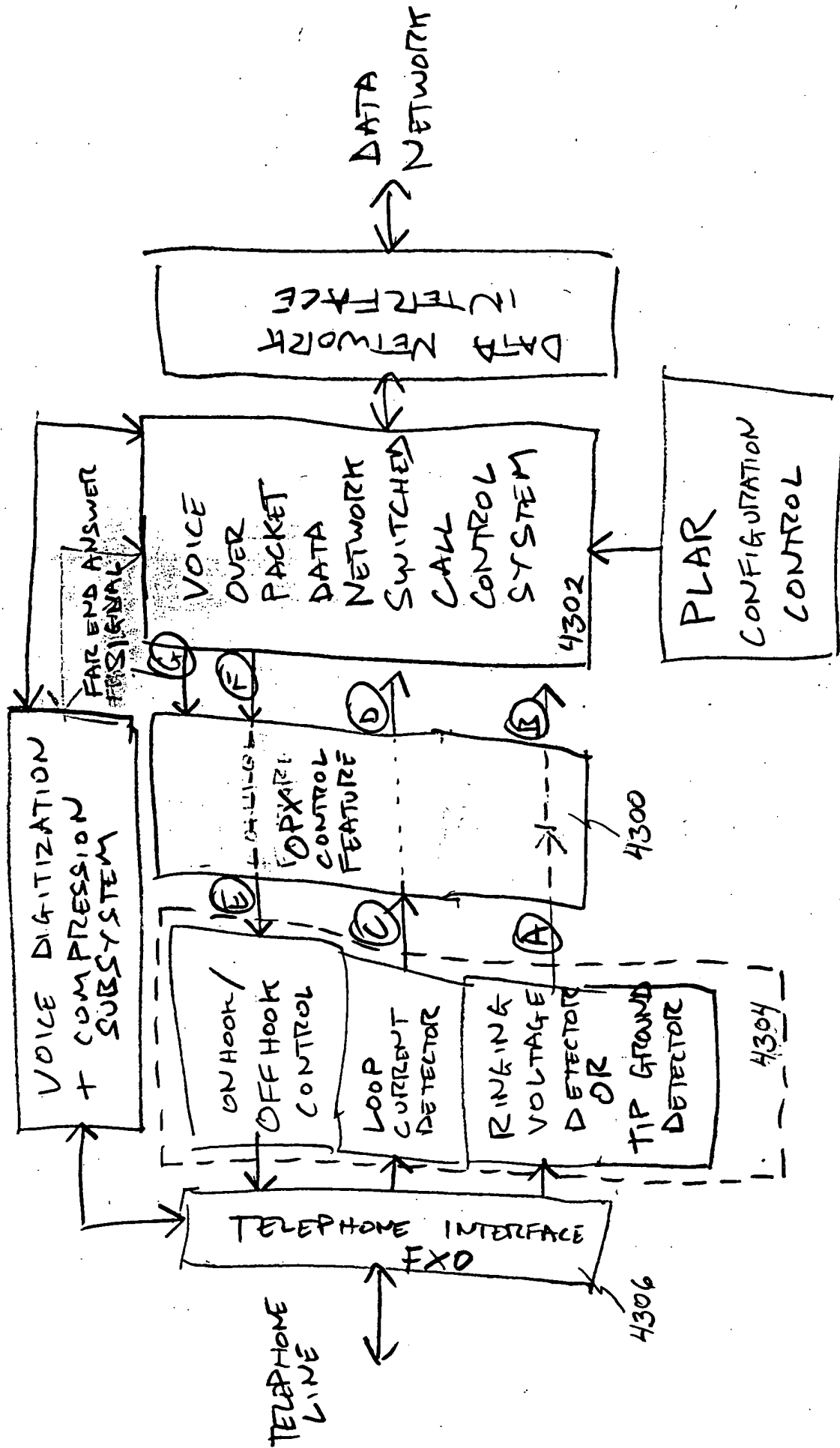


FIGURE 43

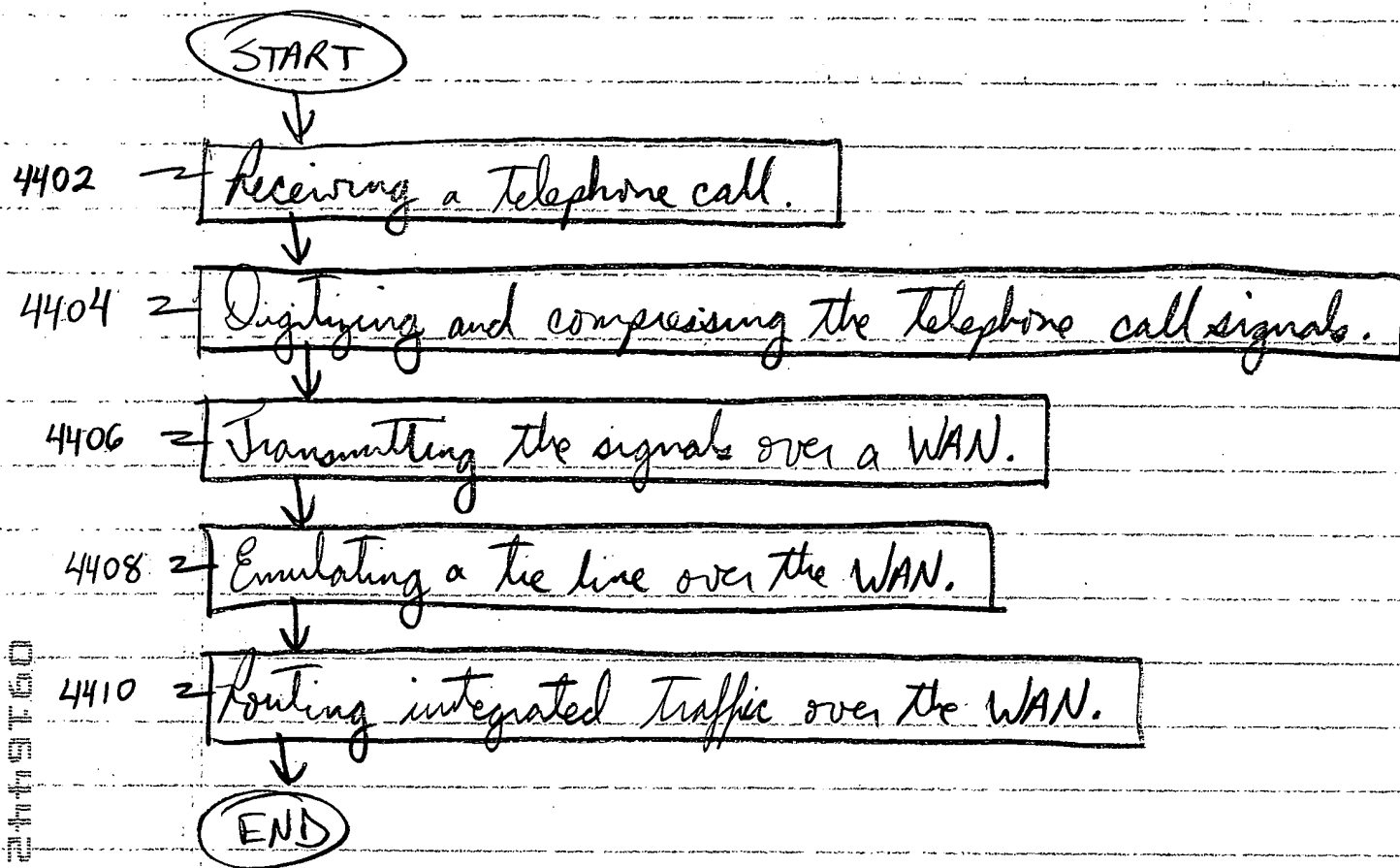


FIGURE 44

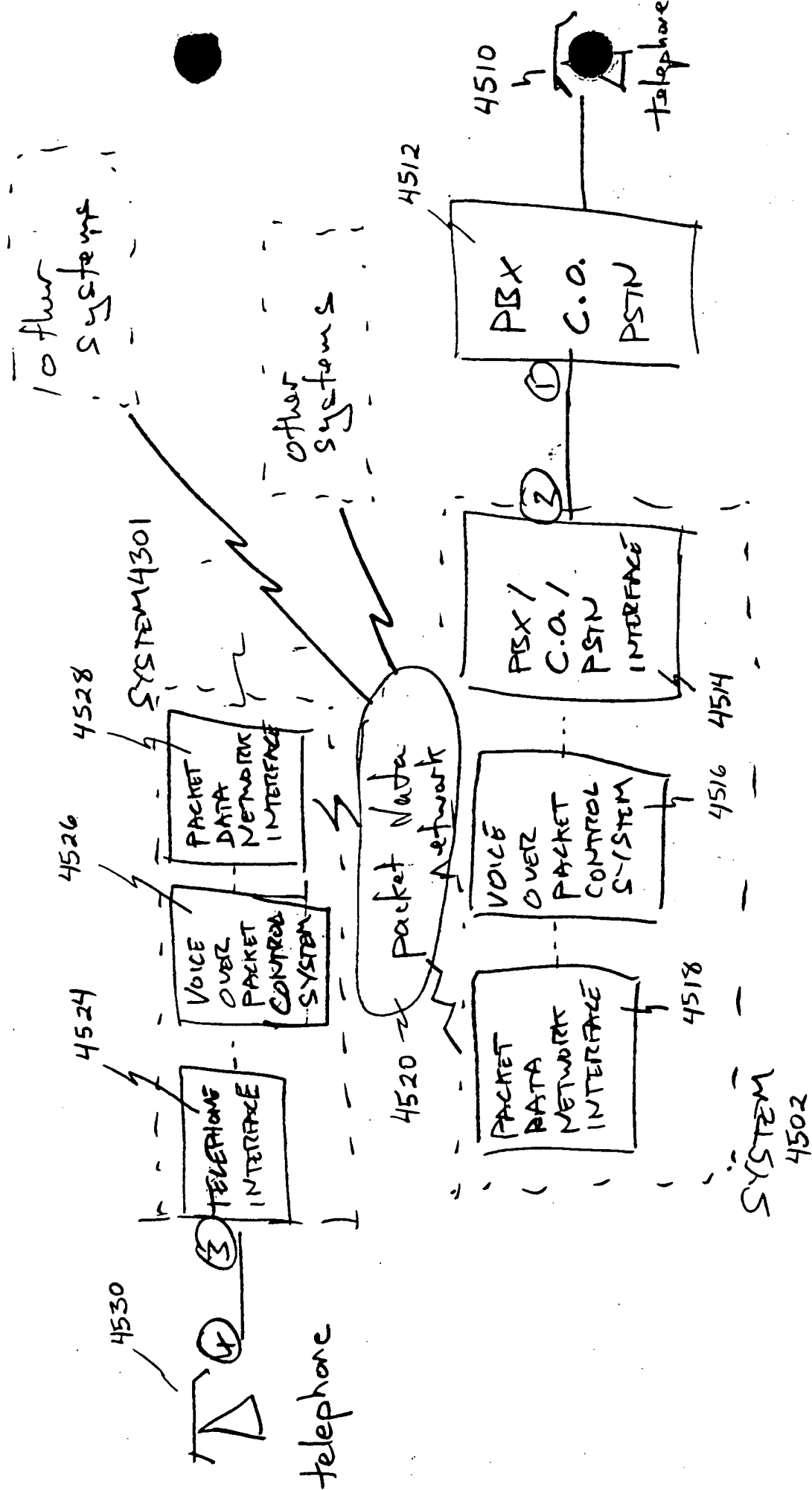


FIGURE 45

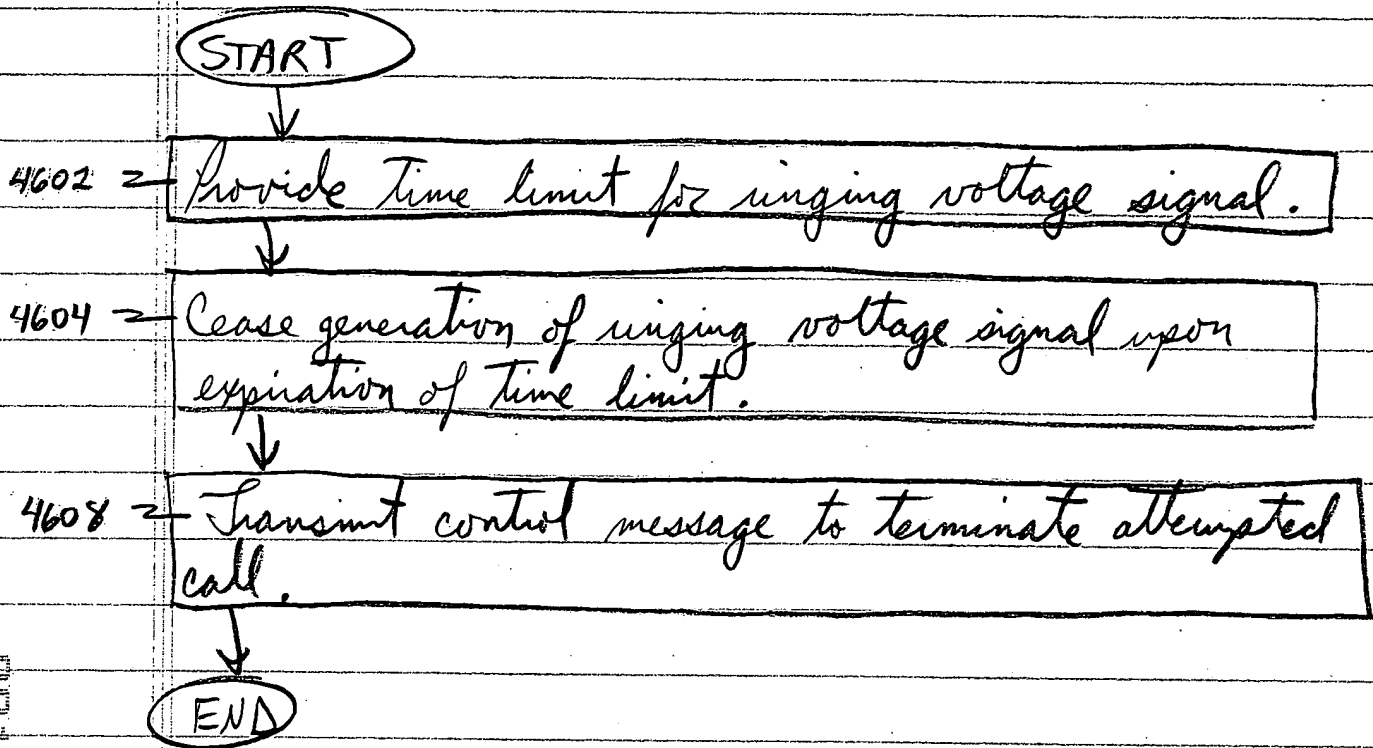


FIGURE 46

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